Towards quantum transport in single-crystalline PbTe nanowire MOSFET devices

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Final version

For my grandparents

Table of natural constants

Planck constant	h	$6.6261 \cdot 10^{-34}$	Js
Planck's constant (reduced)	$\hbar$	$1.0546 \cdot 10^{-34}$	Js
Boltzmann constant	k_b	$1.3806 \cdot 10^{-23}$	J/K
Vacuum permittivity	ϵ_0	$8.8542 \cdot 10^{-34}$	F/m
Vacuum permeability	μ_0	$1.2566 \cdot 10^{-6}$	H/m
Elementary charge	e	$1.6022 \cdot 10^{-19}$	C
Electron mass	m_0	$9.1093 \cdot 10^{-31}$	kg
Bohr magneton	μ_B	$9.2740 \cdot 10^{-31}$	J/T

Abstract

PbTe is a narrow band gap semiconductor with a remarkably high Landé g-factor and spin-orbit interaction. This makes it a very interesting possible candidate for Majorana devices. Therefore the MBE growth of low-defect single-crystalline PbTe nanowires has been developed. This research aimed to develop a fabrication recipe for reliable fabrication of nanowire MOSFET devices. And to use these to characterise the electronic transport properties of these nanowires.
However, Schottky barriers were formed between the nanowire and the Ti/Au source and drain contacts, partially due both the material choice and the fabrication procedure.

The Schottky barriers have been characterised based by fitting the measured transport data with a thermionic emission model. This established thermionic emission as the dominant transport mechanism, and allowed for the determination of the Schottky barrier height ($\Phi_B^{\text{eff}} = 0.55 \pm 0.25$V).
Despite the Schottky barriers, an attempt has been made to extract the carrier mobility and density from the transport data. Carrier densities in the order of $\sim 10^{18}$cm^{-3} have been obtained. This seems a plausible value compared to the carrier densities of other narrow band gap semiconductors (InAs, InSb). The obtained mobilities ($\mu_e = 0.02-0.12$cm^2/Vs) are two orders of magnitude lower than in other semiconductors. However, it was to be expected that the mobility of the device was heavily impacted by the presence of barriers at the contact interface.

PbTe nanowires grown in Eindhoven have been fabricated into similar devices in the Frolov group at the University of Pittsburgh. There cryogenic transport measurements were performed on the devices. The barriers at the metal/semiconductor interface, though much less pronounced, turned the nanowires into nanowire quantum dots. Some curious signatures were observed in the transport characteristics of these dots. Some of these features can be explained to be signatures of Wigner localisation of electrons in the dot. Steps have been made in the full quantum-mechanical modelling of this system, but still a lot of time has to be invested to completely reproduce the experimental results.

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Introduction

Quantum computing is a branch of quantum physics that currently enjoys a lot of scientific and commercial interest. Once physically realised, a quantum computer will be able to harness fundamental properties of quantum mechanics, such as linear superposition and entanglement of quantum states, that are not available to classical computers.
Algorithms that manage to fully utilise these properties could revolutionise our current way of processing and encrypting data. These could significantly speed up certain computations. For example, Shor's prime number factor factorisation algorithm would be exponentially faster than a classical analogue [1]. This would essentially break our current way of encrypting data.
Another application of quantum mechanics is the simulation of systems that themselves are quantum mechanical in nature. Think for example of the development of new medicines, or solving high-temperature superconductivity. The calculation power (or number of bits) that a classical computer would require for the simulation of such a system scales exponentially with the number of degrees of freedom, due to its probabilistic nature. This makes the simulation of larger quantum mechanical models fundamentally impossible using a classical computer. However, Feynman already showed in 1982 that certain many-body quantum Hamiltonians can be simulated exponentially faster on a quantum computer than on a classical computer [2], because the calculations themselves are probabilistic in nature.
However, quantum computers have some issues of their own. The most important is quantum decoherence: the state of a system will only remain in a coherent superposition of states for a finite time. Interactions with the environment may collapse the wave function of a quantum state, thereby destroying the information encrypted in it.
Topological quantum computing proposes to exploit the emergent quasiparticles in many-particle systems to encode and manipulate quantum information. These emergent states are fundamentally non-local in nature, and are therefore immune to the usual (localised) sources of quantum decoherence. This makes topological quantum computing intrinsically fault-tolerant. One theorised realisation of a topological quantum computer is based on Majorana quasiparticles in one-dimensional hybrid semiconductor superconductor systems, see section I-C.
A recently proposed material system that could host these Majorana quasiparticles consists of a lead telluride (PbTe) nanowire with lead (Pb) as a superconductor. This thesis focuses on the electronic characterisation of the semiconductor part of this material system, and explores fundamental challenges in device design and fabrication.

I. Emergent Majorana quasiparticles

First a concise, but complete overview of the relevant Majorana physics will be presented. This should also clarify the requirements for a material system to host Majoranas.

A. Dirac and Majorana: the foundation

In 1928, Paul Dirac's efforts to unify special relativity and quantum mechanics resulted in the now well-known Dirac equation (eq.1), which is the relativistic wave equation for massive spin-$\frac{1}{2}$ fermions:

$$\big(i\hbar\gamma^\mu\partial_\mu - mc\big)\psi = 0, \tag{1}$$

with m the particle mass, and ψ the Dirac spinor fields. Special relativity creeps into this equation through the requirement that the γ^μ-matrices[1] are 4×4 matrices that generate the Clifford algebra [3]:

$$\{\gamma^\mu, \gamma^\nu\} = 2\eta^{\mu\nu}, \tag{2}$$

with $\eta^{\mu\nu}$ the Minkowski metric tensor. This equation yielded a remarkable prediction: the existence of antimatter. The existence of the antiparticle to the electron, the so-called positron, was indeed confirmed only a year later [4].

Antiparticles have the same mass and spin as their "regular" counterparts, but carry a charge of the opposite sign. This implies that neutral particles can be identical to their antiparticles. More formally, this requires that the particle field is equal to its Hermitian conjugate: $\psi = \psi^\dagger$. This can only be true if it is a completely real-valued field.

In 1937, Italian physicist Ettore Majorana had the insight that the solutions to the Dirac equations become real, if the γ^μ-matrices were chosen to be completely imaginary [5]. This can be achieved by defining four alternative $\tilde{\gamma}^\mu$-matrices that satisfy the same anticommutation relations (eq.2) as Kronecker products of the Pauli matrices [3]:

$$\begin{aligned} \tilde{\gamma}^0 &= \sigma_2 \otimes \sigma_1 \\ \tilde{\gamma}^1 &= i\sigma_1 \otimes \mathbb{1}_2 \\ \tilde{\gamma}^2 &= i\sigma_3 \otimes \mathbb{1}_2 \\ \tilde{\gamma}^3 &= i\sigma_2 \otimes \sigma_2 \end{aligned} \tag{3}$$

With these new $\tilde{\gamma}^\mu$-matrices the Dirac equation (eq.1) can be rewritten as the Majorana equation for real fields ϕ:

$$\big(i\hbar\tilde{\gamma}^\mu\partial_\mu - mc\big)\phi = 0, \tag{4}$$

[1] Conventional choice for the matrices γ^μ, with σ_i Pauli matrices, and $\mathbb{1}_2$ the 2×2 identity matrices.

In his honour, particles that satisfy this equation are now known as Majorana fermions (MFs).

These Majorana fermions turn out to be rather elusive, as to date no irrefutable evidence for their existence has been found. In the twentieth century, the concept of Majorana fermions was mostly related to high-energy physics. For example, neutrinos have been speculated to be particles of this kind. However, this has been proven very difficult to verify: neutrinos are extraordinarily weakly interacting particles, making them difficult to detect [3][4].

B. The Kitaev chain

More recently it has been recognised that certain condensed matter systems may also support Majorana fermions as emergent quasiparticles. A toy model that manifests these emergent Majorana fermions, is the Kitaev chain [6].

Consider a chain of N fermions with a spin alignment along the z-axis, and only nearest neighbour interactions. Assuming a ferromagnetic coupling, the ground state of such a system will consists of particles with aligned spins (e.g.: $|\uparrow\uparrow\uparrow\uparrow\uparrow ...\rangle$). An excitation of this system will consist of a single flipped spin (e.g.: $|\uparrow\uparrow\downarrow\uparrow\uparrow ...\rangle$). In second quantisation notation this can be expressed in terms of fermionic creation $c_i^\dagger$ and annihilation c_i operators for an excitation/spin flip at position i:

$$\begin{aligned} \text{Ground state} &= |\uparrow\uparrow\uparrow\uparrow\uparrow ...\rangle = |0\rangle \\ \text{First excitation} &= |\uparrow\uparrow\downarrow\uparrow\uparrow ...\rangle = c_i^\dagger |0\rangle \end{aligned} \tag{5}$$

In this description the spin degree of freedom is entirely redundant, as the nature of the excitation created by $c_i^\dagger$ is not specified in this notation. Therefore this model is known as the spinless fermion chain.

Now we recall that the solutions to the Majorana equation are real fields. In the second quantisation formalism this criterion translates to real-valued Majorana creation and annihilation operators: $\gamma_i = \gamma_i^\dagger$, with $\{\gamma_i, \gamma_j\} = 2\delta_{ij}$. From these requirements it can easily be confirmed that the creation and annihilation operators for (conventional) Dirac fermions can be defined in terms of the Majorana operators:

$$\begin{aligned} c_i &= \frac{1}{2}(\gamma_{i,1} + i\gamma_{i,2}) \\ c_i^\dagger &= \frac{1}{2}(\gamma_{i,1} - i\gamma_{i,2}) \end{aligned} \tag{6}$$

In other words: one conventional fermion can be expressed as a combination of two Majorana fermions.
Kitaev suggested that in a fermionic chain, new fermions $\tilde{c}_i$ can be redefined by combining Majorana operators from adjacent sites:

$$\begin{aligned} \tilde{c}_i &= \frac{1}{2}(\gamma_{i,2} + i\gamma_{i+1,1}) \\ \tilde{c}_i^\dagger &= \frac{1}{2}(\gamma_{i,2} - i\gamma_{i+1,1}) \end{aligned} \tag{7}$$

This reordering is schematically shown in fig. 1.

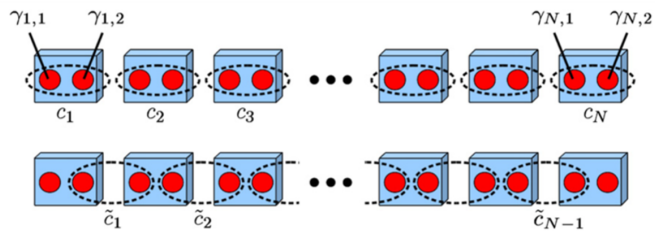


Fig. 1: Schematic depiction of the reordering of the fermionic chain as proposed by Kitaev. The top panel shows a chain of N conventional fermions c_i (blue), and its component Majorana fermions $\gamma_{i,1}$ and $\gamma_{i,2}$ (red). The bottom panel shows the reordering of adjacent MFs into a chain of $N-1$ fermions $\tilde{c}_i$ (dotted ellipses) and the two edge MFs. Reprinted from Leijnse and Flensberg [7].

Now a Hamiltonian for this fermionic chain that only considers nearest neighbour interactions can be defined:

$$\mathcal{H}^{\text{Kitaev}} = -\mu \sum_{i=1}^{N} c_i^\dagger c_i - \sum_{i=1}^{N-1} \left(t c_i^\dagger c_{i+1} + \Delta c_i c_{i+1} + \text{h.c.} \right), \tag{8}$$

with μ the chemical potential, and t the tight-binding interaction strength between neighbouring sites. Notice that the coupling constant Δ between two particles with aligned spins is identified as the superconducting gap. This implies that this Hamiltonian requires triplet Cooper pairing, or p-wave superconductivity.
Consider now the special case $\mu = 0$ and $t = \Delta$. Then the Kitaev Hamiltonian (eq.8) can be rewritten in terms of reordered fermionic operators (eq.7): [7]:

$$\mathcal{H}^{Kitaev} = 2t \sum_{i=1}^{N-1} \tilde{c}_i^\dagger \tilde{c}_i \tag{9}$$

This is just a formal way of reordering the Hamiltonian: it is expressed in a different basis of eigenstates. Notice that this Hamiltonian only counts $N-1$ fermionic states: the two Majorana operators at the ends of the wire ($\gamma_{1,1}$ and $\gamma_{N,2}$) are completely missing. Together these form a highly non-local state: the Majorana zero-mode (MZM):

$$\tilde{c}_M = \frac{1}{2}(\gamma_{1,1} + i\gamma_{N,2}) \tag{10}$$

Because this Majorana zero-mode is not included in the Hamiltonian, it does not cost any energy to occupy this state (hence the name zero-mode). As a result, all the energy states of the Kitaev chain become two-fold degenerate. As will be discussed in sectionI-D, this is essential for the application of MZMs as qubits.
Up until now only the case $\mu = 0$ and $t = \Delta$ was considered, but it can be show that the Majorana edge states remain as long as the chemical potential resides within the gap $|\mu| < 2t$ [6].

C. Physical realisation: semiconductor-superconductor heterostructures

As noted before, the Kitaev model requires p-wave superconductivity to host Majorana edge states. Unfortunately, p-wave superconductors do not exist in nature. However, if a material system can be engineered whose Hamiltonian closely resembles a p-wave superconductor, it may still be able to host a MZM.

In this context, "close enough" means in this context that the Hamiltonian of the material system can be continuously transformed into the Hamiltonian of a p-wave superconductor, without ever closing the superconducting gap [7].
Lutchyn et al.[8] and Oreg et al.[9] proposed that one-dimensional semiconductor-superconductor heterostructures could indeed host MZMs.

Let's start by considering a long and thin nanowire. Electrons in such a nanowire will be strongly confined in the transverse direction when the wire cross-section is small compared to the electron Fermi wavelength. This confinement results in well-separated subbands. Using (local) gates on the wire, conductance channels in the wire can be opened or closed for electronic transport. If only one channel is opened, the wire can effectively be considered as a 1D system [7].
Generally the Hamiltonian of a semiconductor in terms of the fermionic fields $\Psi_\sigma \mathbf{r}$:

$$\mathcal{H}_0 = \sum_{\sigma=\uparrow,\downarrow} \int d\mathbf{r} \Psi_\sigma^\dagger(\mathbf{r}) H_0(\mathbf{r}) \Psi_\sigma^\dagger(\mathbf{r}) \,, \tag{11}$$

where the single-particle Hamiltonian $H_0(\mathbf{r})$ is given by:

$$H_0(\mathbf{r}) = \frac{\mathbf{p}^2}{2m^*} - \mu + \alpha(\mathbf{E}(\mathbf{r}) \times \mathbf{p}) \cdot \bar{\sigma} + \frac{1}{2} g \mu_B \mathbf{B}(\mathbf{r}) \cdot \bar{\sigma} \tag{12}$$

Here m^* is the effective electron mass in the semiconductor, and $\bar{\sigma}$ is a vector of Pauli matrices. The second to last term describes a generic spin-orbit coupling of strength α. $\mathbf{E}$ is the electric field experienced by the electrons. The last term includes Zeeman splitting in the model. $\mathbf{B}$ is an applied field and g is the Landé g-factor.

Superconductivity can be proximity-induced in a nanowire, if a defect-free interface with a superconductor is formed. In this case electrons can tunnel between the two materials. Therefore an electron-electron pairing term with coupling strength $\Delta(\mathbf{r}, \mathbf{r'})$ can be added to this Hamiltonian. The strength of this term depends on both materials, as well as the quality of the interface.
Because of electron-hole symmetry it is conventional to define the Nambu spinors when describing superconducting systems[2]:

$$\bar{\Psi}(\mathbf{r}) = \begin{pmatrix} \Psi_\uparrow(\mathbf{r}) \\ \Psi_\downarrow(\mathbf{r}) \\ \Psi_\downarrow^\dagger(\mathbf{r}) \\ -\Psi_\uparrow^\dagger(\mathbf{r}) \end{pmatrix} \tag{13}$$

Now the eigenspinors of the Bogoliubov-de Gennes (BdG) equation describes quasiparticle excitations in the proximitised system [3]:

$$\bar{H}_0(\mathbf{r}) \bar{\Psi}_i(\mathbf{r}) + \int d\mathbf{r'} \bar{\Delta}(\mathbf{r}, \mathbf{r'}) \bar{\Psi}_i(\mathbf{r'}) = E_i \bar{\psi}_i(\mathbf{r}) \tag{14}$$

[2] Eq.6 (or eq.7) can be rewritten as:

$$\gamma_{i,1} = c_i^\dagger + c_i, \qquad \gamma_{i,2} = i(c_i^\dagger - c_i)$$

From writing the operator expressions in this form, it is apparent that the Majorana operators can be expressed as a superposition of an electron and a hole, reminiscent of a Bogoliubov quasiparticle in a superconductor [7][10].

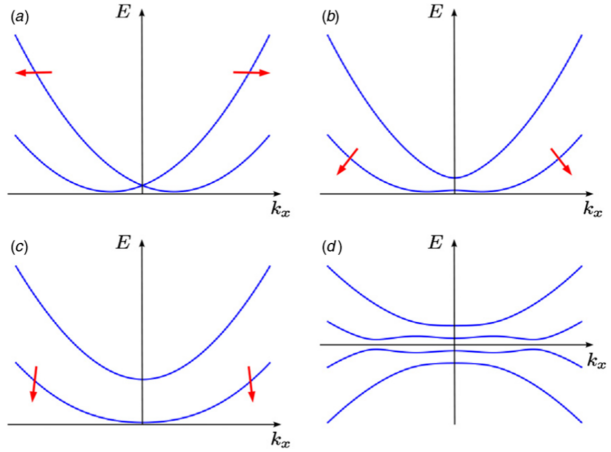


Fig. 2: One-dimensional dispersion relation of a nanowire:
a| with Rashba spin-orbit coupling. This shifts the spin-degenerate subbands along the momentum axis in opposite directions.
b| with an additional (small) magnetic field. The resulting Zeeman splitting lifts the spin-degeneracy and opens the gap at $k_x = 0$.
c| with SOI and a larger magnetic field, which increases the gap and the spin alignment in the subbands.
d| with SOI, an external magnetic field, and proximity-induced superconductivity: these are the dispersion curves are the solution to the Bogoliubov-de Gennes equation. Both the electron and hole bands are plotted here.
Reprinted from Leijnse and Flensberg [7]

Because the Majorana quasiparticles are their own antiparticles $\left(\bar{\Psi}_i^\dagger(\mathbf{r}) = \bar{\Psi}_i(\mathbf{r})\right)$, they can only ever be eigenstates of the BdG-equation at $E = 0$. So in correspondence with the Kitaev model, this physical system can indeed host Majorana zero modes.

Let's now examine the dispersion of electrons in a semiconductor nanowire (fig.2) for a bit more insight of the role of the different components in this Hamiltonian.
In its simplest form, this dispersion takes on the form of a one-dimensional parabola, due to the strong confinement of the electron wavefunctions in the transverse directions. Spin-orbit interaction (SOI) lifts the spin-degeneracy: the two spin-subbands shift in opposite directions along the k_x-axis (see fig.2a) [11].
The addition of a magnetic field perpendicular to the nanowire axis results in Zeeman splitting of the energy bands (see fig.2b). This opens a gap at $k_x = 0$. If the chemical potential is tuned inside the gap, only the bottom band is occupied. This essentially transforms the system to a continuous version of Kitaev's spinless fermion chain [12]. The stronger the applied magnetic field, the wider the area in momentum space that is effectively spinless.

Proximity-induced superconductivity pairs electrons with opposite spin in Cooper pairs. This pairing competes with the Zeeman splitting of the energy bands for the alignment

[3] Here $\bar{H}_0(\mathbf{r})$ and $\bar{\Delta}(\mathbf{r}, \mathbf{r'})$ are the 4×4 extensions of the 2×2 single-particle Hamiltonian and pairing potential matrices, respectively:

$$\bar{H}_0(\mathbf{r}) = \begin{pmatrix} H_0(\mathbf{r}) & \hat{0} \\ \hat{0} & -\sigma_y H_0^*(\mathbf{r}) \sigma_y \end{pmatrix}, \qquad \bar{\Delta}(\mathbf{r}, \mathbf{r'}) = \begin{pmatrix} \hat{0} & \Delta(\mathbf{r}, \mathbf{r'}) \hat{1} \\ \Delta(\mathbf{r}, \mathbf{r'}) \hat{1} & \hat{0} \end{pmatrix}$$

of the spins in the nanowire [12][13].
For weak magnetic fields the superconducting pairing will dominate; the nanowire will behave as a trivial s-wave superconductor. This dispersion will still display a gap, but this is merely the conventional superconducting gap. If the Zeeman splitting dominates, a topological phase transition takes place (the bands invert), and the topological gap opens up. Electrons are now still paired, but with aligned spins: the system is in a p-wave superconducting state. So the nanowire is in the topological state if:

$$\frac{1}{2}g\mu_B B \geqslant \sqrt{\mu^2 + \Delta^2}\,. \tag{15}$$

When only a part of the nanowire is proximitised by a superconductor, also only the covered part can be in the topological state. Because the bands are inverted in the topological state, there has to be a point where the bands cross when moving from the trivial to the superconducting regions in the wire. Because electron-hole symmetry in superconductors, this crossing has to occur exactly at zero energy. This is where the Majorana zero mode can occur: at the interface between the trivial and superconducting regions. Therefore it is also known as a Majorana edge mode.

From this discussion a short list with requirements for a device that can host MZMs can be made:

1) A low-defect 1D (nanowire) semiconductor material
2) Strong Rashba spin-orbit interaction
3) Large Landé g-factor
4) Proximity-induced superconductivity
5) Global and local gates to tune the chemical potential into the topological gap.

This list will be used for further discussions of suitable material combinations and device designs.

For a more formal description of discussion above, the review papers by Leijnse and Flensberg [7], Alicea [14], and Aguado [15] are highly recommended.

D. Majorana's for quantum comupting

The fundamental building block of a quantum computer is the quantum bit (qubit). It has been proposed that so-called Majorana qubits can be created based on these Majorana zero-modes. Operations can be performed on such a qubit based on its exchange statistics. When two bosons (fermions) exchange positions, the total system acquires a phase factor of +1 (-1). However, MZMs are non-Abelian anyons [16]. This means that the phase factor the system acquires upon the exchange of two MZMs depends on the path taken. Moreover, if multiple operations are performed in succession, the accumulated phase factor also depends on the order of the operations. Therefore information can be encoded in the phase of the Majorana qubits, by exchanging the positions of the MZMs [17][18]. This process is called braiding.
Because the MZMs are highly non-localised emergent quasi-particles, the Majorana qubits based on them are very robust to local perturbations: they are topologically protected [19]. Therefore computation operations are inherently fault tolerant.

II. PbTe versus the status quo

Here a short overview of the state-of-the-art experiments and material systems used for the detection of MZMs will be given. This will be compared to the PbTe/Pb material system. From this comparison the motivation for this project should become clear.

A. Experimental signatures of Majorana fermions

Since the theoretical prediction in 2001 by Kitaev [6], significant steps have been undertaken to experimentally verify the existence of MZMs in condensed matter systems. The first signature, the zero-bias conductance peak, was reported by Mourik et al. in 2012 [13]. However, to date no conclusive evidence for their existence has been presented.

The detection scheme used by Mourik et al. and numerous experiments since then [20][**?**][21], is based on tunneling spectroscopy (see fig.3). In these devices a nanowire is placed on a substrate with back gates. These gates can be used to tune the Fermi level in the wire into the topological gap. Two contacts are deposited onto the wire: a superconducting contact, and a conventional Ohmic contact. A separate back gate can be found underneath the part of the wire that is covered by neither of the contacts. If a negative voltage is applied to that gate, a tunnel barrier for electrons is formed between the topological region and the Ohmic comtact.
When a magnetic field is applied, Majorana zero modes are formed at the edges of the topological region (indicated in pink in fig.3a). If a bias voltage is applied between the two contacts, tunneling through the barrier can occur. This is shown as a waterfall plot in fig.3b for various magnetic field strengths. Here the emergence of the Majorana zero mode (MZM) as a function of the applied Zeeman field can be seen as a zero-bias conductance peak. For low fields the topological gap is closed, and thus no MZM is permitted. If the applied field is high enough to open the gap, the in-gap states clearly emerge at zero bias, giving rise to a conductance peak.

However, all signatures of Majorana fermions measured to date are no definitive proof for their existence. For example, in the case of the experiment by Mourik et al. the zero-bias peaks do not have the predicted amplitude of one conductance quantum: $G_0 = \frac{2e^2}{h}$. Several other phenomena have been proposed that can show similar signatures: Andreev bound states, weak antilocalisation, and the Kondo effect [20][21]. Braiding experiments can reveal the non-Abelian properties of the Majorana fermions, and thus ultimately proof their existence [17][22].

B. PbTe vs InAs and InSb

Several material systems have been proposed as physical realisations of the semiconductor-superconductor heterostructure discussed in sec.I-C. Most notably indium arsenide (InAs) or indium antimonide (InSb) nanowires with aluminium as a superconductor. Both semiconductor materials have a large Landé g-factor, which requires lower

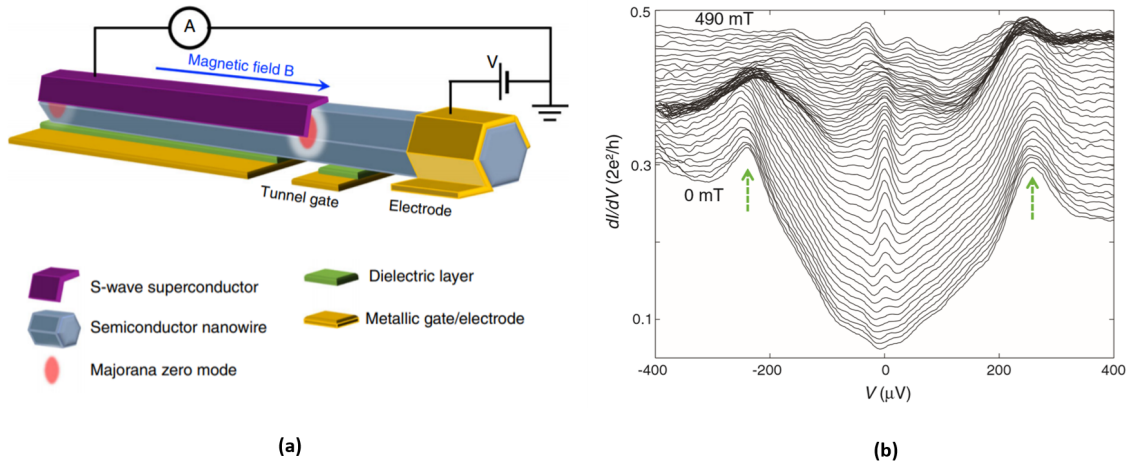


Fig. 3: **(a)** Schematic depiction of the device used to detect the Majorana zero modes. A nanowire is contacted with a normal and a superconducting contact, over which a voltage is applied and the resulting current measured. A global gate underneath the superconducting region can be used to tune the Fermi level to be in the topological gap. The local tunnel gate can be used to either tune the number of open conduction channels in the wire, or form a tunnel barrier. Reprinted from Zhang et al. [21].
(b) Waterfall plot of the measured conductance (dI/dV) as a function of the applied bias voltage and the applied magnetic field. It can clearly be seen that zero-bias peaks get formed when the applied magnetic (Zeeman) field is high enough to open the topological gap. Reprinted from Mourik et al. [13].

magnetic fields to open the gap. This is important because the magnitude of the applied magnetic field is limited by the critical field of the superconductor. Both materials also have a large spin-orbit strength, which leads to more pronounced subband splitting.

However, the previous section ended with a short discussion on why the existence MZMs of has not yet irrefutably been proven. Most of the state-of-the-art experiments up until now have been performed with either InAs or InSb nanowires. Therefore another material system has been proposed: lead telluride nanowires with superconducting lead. A comparison between the three semiconducting materials is shown in the table below:

Material	**InAs**		**InSb**		**PbTe**	
Bandgap (eV at 300K)	0.35	[23]	0.18	[23]	0.31	[23]
Landé g-factor	20-50	[24]	58-64	[25]	66	[26]
Spin-orbit energy (μeV)	10	[24]	230	[27]	330	[28]
Electron mobility (cm$^2/V$sat 4.2K)	$3.3 \cdot 10^4$	[29]	$7.7 \cdot 10^4$	[30]	-	

PbTe is predicted to have an even higher g-factor than both InAs and InSb. Moreover, experiments on PbTe wires used for this project have already shown that the spin-orbit interaction in these wires is stronger than in the InAs or InSb nanowires used in the leading experiments performed in the last decade [28].

Another big advantage of PbTe over the other two materials is the pairing with the superconductor. Diffusion of aluminium atoms into the InAs or InSb nanowire reduces the quality of the interface between the superconductor and the nanowire. Lead can be grown approximately lattice matched with the PbTe nanowire [26], and diffusion of lead into PbTe does not pose an issue. Therefore this material system is more likely to produce a clean interface, and therefore a hard superconducting gap.

III. Structure of this thesis

This work focuses on the characterisation of the (quantum) transport properties of MBE grown PbTe nanowires, and works towards their application in Majorana devices. Therefore three main goals are set:

- Develop devices that allow transport measurements to be performed on the PbTe nanowires.
- Characterisation material properties (carrier mobility and density, band gap, g-factor) and compare to InAs and InSb.
- Achieve reliable tunability of the carrier concentration by controlling the IV/VI ratio during growth.

Chapter 2 elaborates on the material properties of PbTe, and on the nanowire growth. This will be followed by a discussion on transport phenomena in semiconductor materials and the working principles of MOSFET devices in chapter 3. Next, chapters 4 and 5 explain the practical matters of the device fabrication and measurement procedures. After which the results of this project are discussed in chapter 6.
During this project, quantum transport measurements were done in Sergey Frolov's group at the University of Pittsburgh on similar devices with the same PbTe wires from Eindhoven as were used in this project. There some interesting and unexpected results were found: a quantum dot was formed in the wire, and it was found that spin blockade was a stronger effect than Coulomb blockade in transport measurements. Chapter 7 explains a (partially finished) fully quantum mechanical model to explain these results.
Finally, chapter 8 will present some concluding remarks, and some follow-up experiments will be proposed.

PbTe nanowires

Lead telluride (PbTe) is a group IV/VI semiconductor material. Even though PbTe/Pb has only recently been proposed as a suitable material system for Majorana devices, PbTe has been extensively studied for other applications. Due to its small direct bandgap, a lot effort has been put into the study of its optical properties for photodetectors [31][32][33]. The thermodynamic properties of PbTe have also been studied elaborately for application in thermoelectric devices [34].
This chapter will go over the relevant material properties for our purposes (section I), and then briefly go over the nanowire growth (section II).

I. PbTe: Material properties

Like most lead chalcogenides, PbTe crystallises in the rock salt crystal structure [23]; this is shown schematically in fig.4a. This crystal structure can also be viewed as two interpenetrating FCC sublattices: one sublattice for each element. The bonds between the atoms have a mixed covalent-ionic character, with an ionicity $f_i = 0.65$ [35][36].

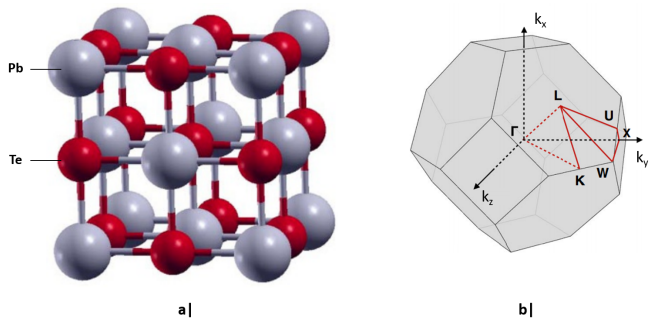


Fig. 4: Sketches of **a**| the crystal structure (adapted from [37]), and **b**| the first Brillouin zone (reprinted from [38]) of PbTe.

The first Brillouin zone is depicted in fig.4b. The most important symmetry points in reciprocal space have been indicated. PbTe has a narrow direct bandgap at the L-point, as can be seen in fig.5. At room temperature (300K) the bandgap is $E_g = 0.32eV$, and it decreases with temperature to $E_g = 0.18eV$ at 10K [23].

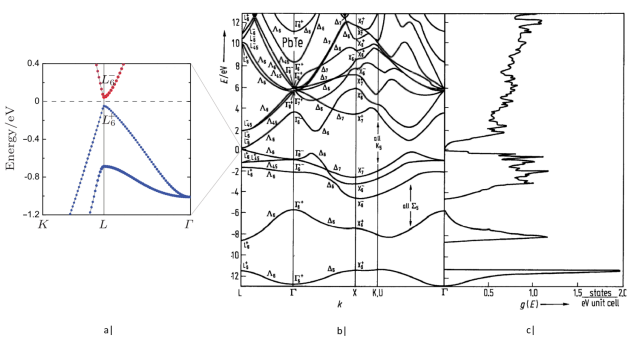


Fig. 5: Band structure of PbTe:
a| Close-up of the band structure of PbTe around the direct bandgap at the L-point. Calculated using DFT by Wang et al.[39].
b| Full band structure and **c**| density-of-states of PbTe, reprinted from [40].

From experiments it has been reported that PbTe can be doped to be either p-type or n-type [41][42]. Native point defects are important doping mechanisms as these have quite low formation energies in PbTe [43]. Depending on how far the crystal deviates from stoichiometry, there are three possible defect states with the lowest formation energy (see fig.6:

- V_{Te}^{2+}: In a Pb-rich crystal, Te vacancy has the lowest formation energy.
- V_{Pb}^{2-}: If the crystal is slightly Te-rich, the Pb vacancy has the lowest formation energy.
- Te_{Pb}^{2+} From DFT calculations Wang et al.[43] that the Te_{Pb}^{2+} antisite defect has the lowest formation energy for highly Te-rich crystals. In this defect type a tellurium atom replaces a lead atom in the crystal lattice.

If the dominant dopant is positively (negatively) charged, the intrinsic Fermi level is shifted towards the conduction (or valence) band, respectively. Therefore a PbTe crystal can be tuned from n-type to p-type and again to n-type by tuning the stoichiometry from Pb-rich to Te-rich [38][43][44][45].

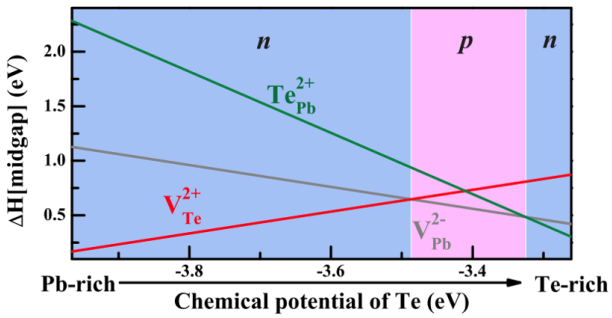


Fig. 6: Midgap formation energy for the three lowest-energy defect states as a function of the chemical potential of Te. The lowest energy defect state determines the doping character of the crystal (blue: n-type, pink: p-type). As calculated by Wang et al.[43].

A last material property PbTe that is relevant to mention, is its high (low-frequency) dielectric constant ($\epsilon(0) = 400$)[23][46]. This results in strong Debye shielding of charged impurities in the PbTe nanowire, or at its interfaces with other material.

II. Nanowire growth

A myriad of chemical methods have been used to synthesise PbTe nanowires, such as electrodeposition , chemical vapour deposition and the chemical vapour transport method [47][48][49][50][51][33]. Especially this last method has yielded wires with good crystallinity and transport properties [52].

Molecular beam epitaxy (MBE) has been reported to yield defect-free PbTe thin-films [53][54]. This can be achieved by using ultrapure sources for the deposition of thin films under ultra-high vacuum (UHV) conditions. Consequently, films grown using MBE have been shown to yield significantly higher carrier mobilities than the chemical methods for wire growth [48][51][54]. Moreover, these reports show control over the intrinsic doping by changing the IV/VI (Pb/Te) flux ratio during the growth process. This determines the deviation from stoichiometry of the grown thin-film and therefore its doping character.
It would be desirable to harness the properties of MBE growth for nanowires as well. Some work has been published on MBE growth of PbTe nanowires [55][56], which shows defect-free, but quite short (several 100 nm) and tapered nanowires.

The nanowires used in this project were grown at the NanoLab@TU/e clean room at Eindhoven University of technology. These wires are single-crystalline, and significantly longer than the ones reported in other works (on average 2-3 μm [26]). In the rest of this section, we will take a closer look at the growth mechanism and quality of these wires.

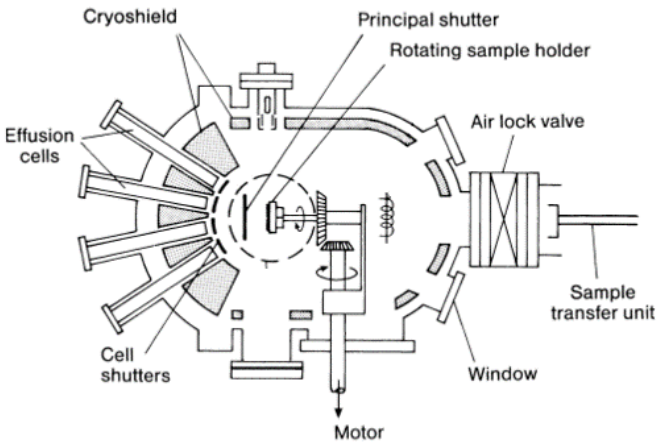


Fig. 7: Schematic depiction of a MBE system. Indicated are its most important component parts. Adapted from Ibach and Lüth [57]

The concept of a MBE system is quite simple. For a schematic depiction of an MBE system, see fig.7. A substrate is placed on a sample holder in an ultrahigh vacuum (UHV). Multiple effusion cells are positioned opposing the sample. The (precursor) material in these effusion cells is evaporated, and will propagate in to the chamber once the shutters are opened. Due to the quality of the UHV and the pressure gradient between the effusion cell and the UHV chamber, the substrate is bombarded by a ballistic beam of the precursor material(s) [57]. A film is deposited on the substrate, if the incoming flux is larger than the re-evaporation rate. Herein substrate temperature is an important parameter. The composition of the grown film can be controlled by the ratio of the incoming fluxes of the precursor materials.

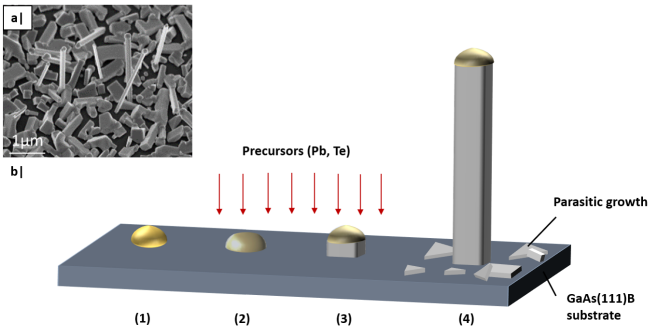


Fig. 8: VLS growth of PbTe nanowires.
a| Inset: SEM image of PbTe nanowires grown using this growth mechanism. It can clearly be seen that the growth yields both nanowires and quite some parasitic growth on the substrate.
b| Schematic representation of the VLS mechanism of nanowire growth:
(1) Catalytic gold droplets are patterned on the GaAs(111)B substrate.
(2) Once the shutters are opened the substrate is bombarded with precursor material.
(3) This precursor material favours the formation of an alloy with the gold droplet over lateral film growth. Supersaturation of the gold droplet with the precursor results in nucleation an growth of the nanowire.
(4) The growth catalysed by the alloy droplet results in wires that are much taller than the surrounding parasitic lateral growth.

The vapour-liquid-solid (VLS) mechanism [58] was used to grow gold-catalysed nanowires on GaAs(111)B substrates (see fig.8b). The gold droplets are pre-patterned onto the substrate using EBL en e-beam evaporation. During the growth process in the MBE system the precursor material (atomic Pb and Te) favours the formation of an alloy with the gold droplet over the nucleation of lateral film growth. Supersaturaton of the alloy droplet with the precursor material will lead to crystalline PbTe deposition under the droplet, lifting it up in the process. This process does not prevent lateral film nucleation and growth, but it does catalyse the wire growth.

Dependent on the growth conditions the wires grow up to 3 μm long, and have diameters of 80-120 nm [26]. In figure 9a a bright-field TEM image shows part of one of the PbTe nanowires. From the electron diffraction pattern (fig.9b) and close-up HAADF-STEM (fig.9c), it can be seen that the wires are indeed single-crystalline and defect-free. Figure 9d shows a close-up image of the top of a wire with the gold droplet. The composition of the wire and the catalytic gold droplet can be seen in the EDX maps shown in figures 9e-h.
From both the EDX maps and the close-up HAADF-STEM it can be seen that a native oxide with a thickness of a few nanometers is formed on the wires upon contact with air.

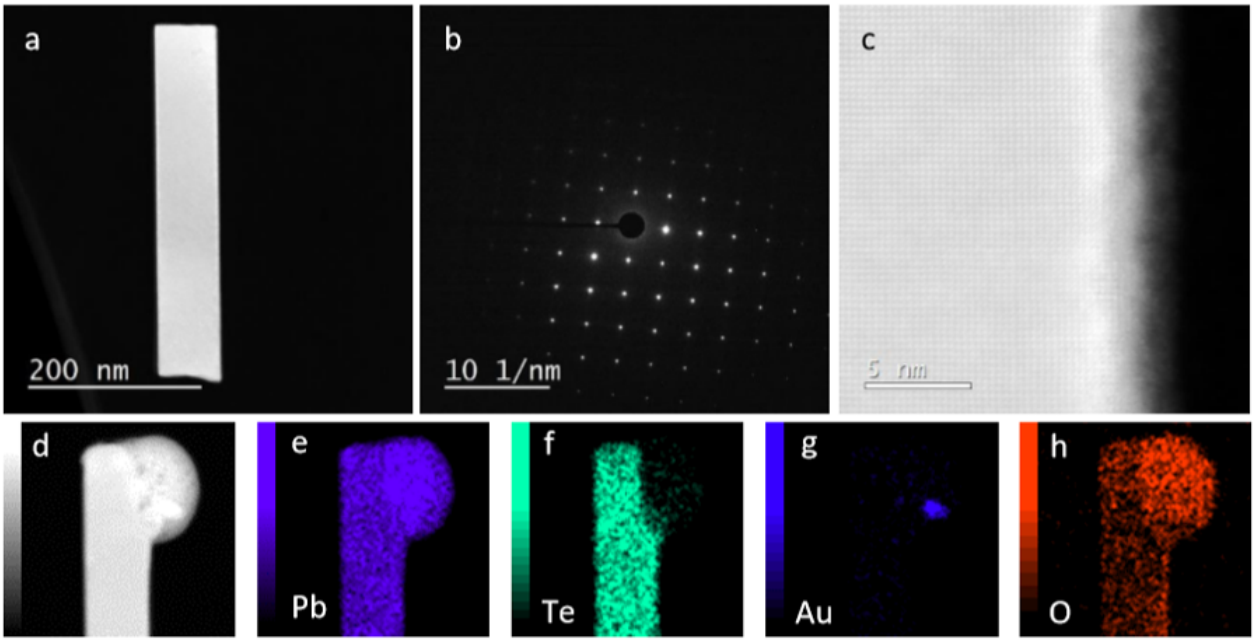


Fig. 9: **(a)** Bright field TEM image of a part of a MBE grown PbTe nanowire. **(b)** Electron diffraction pattern of the same nanowire. **(c)** HAADF-STEM image of the side of the nanowire. **(d)-(h)** EDX mapping Reprinted with permission from A.G. Schellingerhout [26].

Nanowire MOSFET devices

The electrical properties of the PbTe nanowires are determined in field-effect measurements. To be able to perform these measurements, nanowire metal-oxide-semiconductor field-effect transistors (MOSFETs) are fabricated. In this chapter the working principles of these MOSFET devices will be explained. Working towards that goal, first the electric properties of semiconducting materials themselves will be discussed (section I). Then the interfaces between semiconductors and other materials will be described (section II). This is important to understand the influence of the contacts on the carrier transport through the device. Finally, the working principles of nanowire MOSFETs (section III will be explained. Some extra attention will be given to non-ideal behaviour, such as capacitance effects and subthreshold conduction.

I. Electronic properties of semiconducting materials

Before the entire device geometry is discussed, we will first take a look at the electronic properties of a (bulk) semiconductor material.

A. Carrier densities

In an undoped (intrinsic) semiconductor the chemical potential μ is lies at the centre of the band gap. This position is called the intrinsic Fermi level $E_{F,i}$. In such a material free charge carriers can only be created by means of thermal or optical excitation over the band gap. Such an excitation creates an electron-hole pair: an electron in the conduction band, and a hole in the valence band. In a similar process, an electron can relax back to the valence band and recombine with a hole. In this process energy is conserved through the emission of phonons and/or photons.
In thermal equilibrium, the excitation rate is equal to the recombination rate. This implies that the electron density ρ_n and hole density ρ_p are also equal. Therefore the intrinsic carrier density ($\rho_i = \rho_n = \rho_p$) can be expressed as:

$$\rho_i = \sqrt{N_c N_v} \exp\left(\frac{-E_g}{2k_b T}\right) , \tag{16}$$

with N_v and N_c the effective density of states in valence and conductance bands, respectively. Here E_g is the band gap energy, and T the temperature.

The carrier density can be modified by introducing dopants to the material. These dopants are electrically active impurities, that either introduce additional electrons or holes to the system [57]. Donor states introduce extra electrons to the system. This results in $\rho_n > \rho_p$, therefore this is called an n-type semiconductor. The addition of electrons increases the radius of the Bloch sphere. Therefore the Fermi level shifts towards the conduction band.
Acceptor states capture an electron from the valence band. This is equivalent to the introduction of extra holes. In such a p-type material the Bloch sphere shrinks due to the dopants, and the Fermi level will shift closer to the valence band.
Fig.10 shows the (inverse) temperature dependence of the electron density in a n-type semiconductor. A similar curve can be sketched for holes in a p-type material. The temperature dependence can be divided into 4 different regimes:

- At very low temperatures, the extra electron/holes are bound to the donor/acceptor states. This is called the freeze-out regime: doping does not contribute to the carrier density, and also the intrinsic carrier density is negligible. The material behaves as an insulator.
- If the thermal energy is larger than the activation energy E_A needed to ionise the donors/acceptors, the carrier density will increase with temperature. This is called the ionisation regime: the majority carrier density can be described using an Arrhenius equation [59]:

$$\rho_{n/p} \propto \exp\left(\frac{-E_A}{k_b T}\right) \tag{17}$$

- The saturation regime is a temperature range where all donors/acceptors are ionised, but the contribution of the intrinsic carriers is still exceedingly small. The carrier concentration is approximately constant.
- Finally, at relatively high temperatures thermal excitation of intrinsic carriers starts to contribute significantly to the total carrier density.

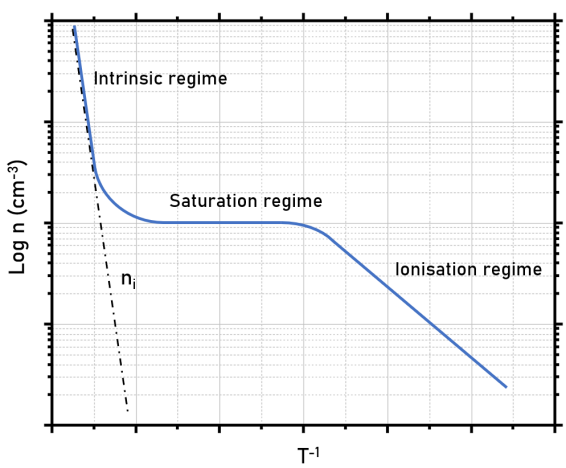


Fig. 10: Electron density as a function of inverse temperature. Indicated are the intrinsic, saturation, and ionisation regimes. The dotted line indicates the temperature dependence of the carrier density for an intrinsic semiconductor.

B. Electronic transport

Electronic transport is defined as the net flow of carriers under the influence of an electric field (drift) or a gradient in the carrier concentration (diffusion) [60]. In the nanowire MOSFET devices we consider here the field-driven current dominates [61]. The electronic current density is given by:

$$J_n = -e\rho_n v_d \,, \tag{18}$$

with v_d the drift velocity. This drift velocity is the average electron velocity, and is limited by scattering.
If only drift due to an electric field E is considered, the generalised force on an electron is given by:

$$m_e^* \frac{dv}{dt} = -eE \,, \tag{19}$$

with m^* and v the effective mass and velocity of an electron, respectively. In a steady-state approximation, this reduces to an equation for the drift velocity:

$$v_d = -eE\tau/m_e^* \,, \tag{20}$$

here τ is the average time between scattering events. This scattering term limits the drift velocity. Here the electrons were considered as the majority carriers; a similar equation can be written down if holes are the majority carriers.

By combining equations 18 and 20, the current density can be expressed as a function of the applied electric field:

$$J = \sigma E \,, \tag{21}$$

where the conductivity σ is defined as:

$$\sigma = -e\rho_n\mu_n + e\rho_p\mu_p \,. \tag{22}$$

Here the actual response to the electric field is given by the carrier mobilities $\mu_{n/p}$:

$$\mu_{n/p} = e\tau/m_{n/p}^* \,, \tag{23}$$

The carrier mobility is again limited by scattering. The dominant scattering processes are impurity and electron-phonon scattering [59][62][63][64]. The electron-phonon scattering cross-section decreases with temperature, leading to a significant increase in carrier mobility [**?**].

II. Metal-semiconductor interfaces

The interfaces between different materials have an important effect on the transport of charge carriers through electronic devices. In this section the physics of material interfaces and the consequences for electronic transport will be discussed.

A. The Schottky-Mott model

The simplest model to describe the potential landscape for free charge carriers at an interface between two materials is the Schottky-Mott model. This model describes the alignment of the valence band maxima (VBM) and conduction band minima (CBM) between the two materials, based on a simple assumption: the system is in thermal and electrostatic equilibrium. In other words: no spontaneous currents flow through the system.

The energy bands of an isolated metal and an n-type semiconductor are shown in fig.11a. Both are aligned to the vacuum level. If the two materials are brought into contact, the Fermi level difference will induce the exchange of charge between the materials. This results in the build-up of a space-charge region at the interface. The potential drop over this interface compensates for the Fermi level difference, resulting in a system that is in electrostatic equilibrium. This band bending is shown in fig.11b.
The band bending results in an asymmetric potential barrier for electrons at the interface. The barrier the electrons encounter when moving from the metal into the semiconductor is called the Schottky barrier Φ_B. This barrier height is defined solely by the work function of the metal ϕ_m and the electron affinity of the semiconductor χ_{sc}:

$$\Phi_B = \phi_m - \chi_{sc} \tag{24}$$

The built-in potential V_{bi} is the (unbiased) potential for electrons moving out of the semiconductor:

$$eV_{bi} = e\Phi_B - (E_F - E_c(bulk)) \,. \tag{25}$$

This potential is a function of the distance between the Fermi level and the conduction band, and therefore depends on the doping density. The potential barrier (ΔV) an electron

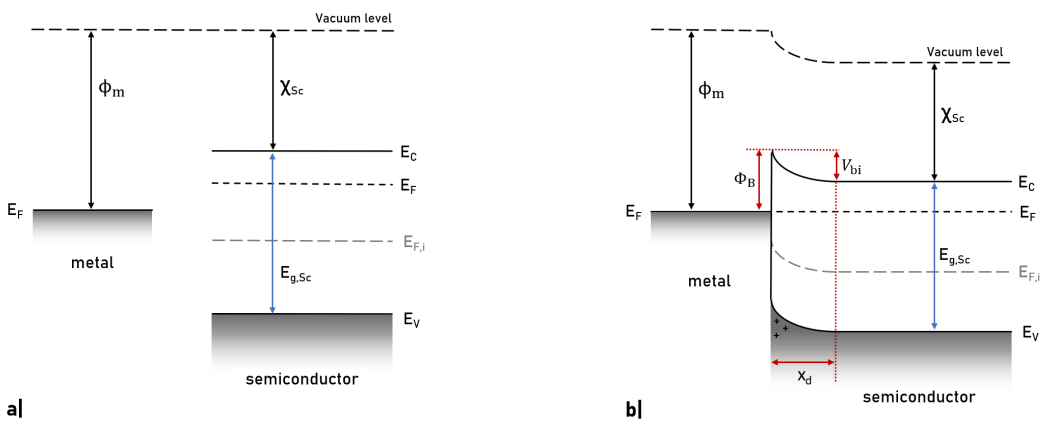


Fig. 11: Energy band alignment at a metal-semiconductor interface for a n-type semiconductor.
a| Energy bands of the isolated metal and semiconductor aligned to the vacuum level. Specified are the metal work function ϕ_m and the semiconductor electron affinity χ_{sc} and band gap $E_{g,sc}$.
b| Band bending at a metal-semiconductor interface. Here also the Schottky barrier height Φ_B and built-in potential V_{bi} are indicated in red.

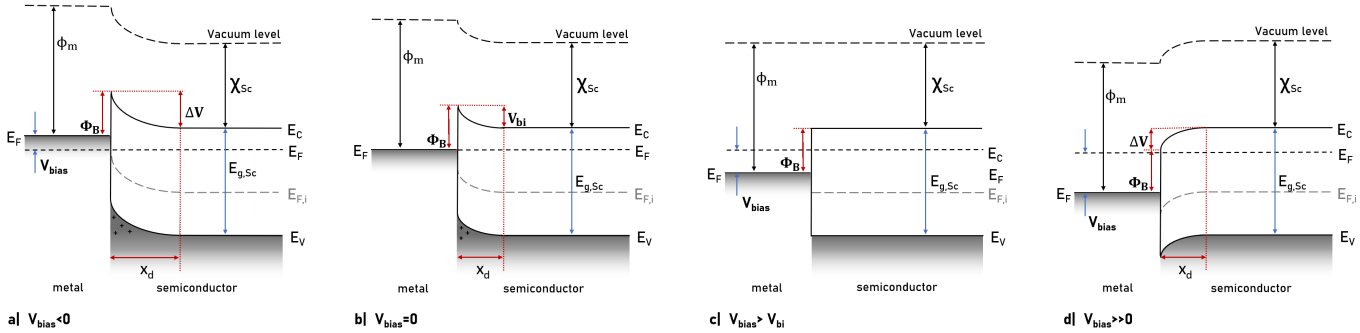


Fig. 12: The influence of a bias voltage on a Schottky contact:
a| $V_{\text{bias}} < 0$: Backward bias. **c**| $V_{\text{bias}} = V_{bi}$: Flat-band bias.
b| $V_{\text{bias}} = 0$: No bias. **d**| $V_{\text{bias}} >> 0$: Large forward bias

encounters when moving out of the semiconductor can be influenced by applying a bias voltage over the junction. Per definition, at zero bias this potential is equal to the built-in potential. A positive (forward) bias decreases the barrier height, and a negative bias enlarges the barrier height. This is shown for the hypothetical barrier discussed before in fig.12. For certain bias voltages ($V_{\text{bias}} > V_{\text{bi}}$) an electron current can flow unimpeded from the semiconductor into the metal, but encounters a barrier the other way around: the metal-semiconductor interface forms a rectifying contact.

The specific band alignment shown in fig.12 results in the formation in Schottky contacts. However, for other material combinations another type of contact can be formed: the Ohmic contact. An Ohmic contact is defined to have a resistance that is negligibly small for a current in both directions, compared to the resistances of the materials themselves [65]. In practice a contact shows Ohmic behaviour, if the barrier height can be overcome by the thermal energy of the charge carriers (0.9 mV at 10K, 25.9 mV at 300K).
Ohmic contacts can be realised in two ways:

- If the semiconductor is heavily n-doped (p-doped), the Fermi level is positioned very close to the CBM (VBM). The resulting band bending is shown in fig.13a. This alignment creates a tunnel barrier at the interface that is approximately equal for charge carriers moving in both directions: $\Phi_B \approx V_{bi}$. The large doping density also effectively screens the bulk of the semiconductor from the metal. Therefore the depletion region will be fairly narrow, resulting in an effective tunnel barrier.
- All sketches shown in fig.11b, fig.12, and fig.13a show the formation of Schotkky barriers. All have in common that the work function of the metal is larger than the work function of the semiconductor. When the effect of surface states is ignored, this will always result in the formation of Schottky barriers in the conduction band. The opposite case will result in the formation of an Ohmic contact, as is sketched in fig.13b. In general, Schottky barriers form for n-type and p-type under conditions summarised in the table below:

	n-type	p-type
$\phi_m > \phi_{sc}$	Schottky	Ohmic
$\phi_m < \phi_{sc}$	Ohmic	Schottky

The Schottky-Mott model is actually a quite naive description of an interface, as it only describes how bulk properties are modified near the interface. But it completely ignores any effect the surface itself may have. Therefore the contribution of intrinsic surface states, trapped charges, and other interface effects will be discussed in sec.II-C.

B. *Mechanisms of electronic transport*

Let us now consider a typical n-type Schottky barrier as depicted in fig.12. Two mechanisms contribute to the transport of electrons across such a barrier: field emission (tunneling) and thermionic emission.

Field emission: Field emission is the thermally-assisted tunneling of charge carriers through the (rounded) triangular barrier created by the band alignment [65][66]. This tunneling process is also known as Fowler-Nordheim tunneling. The tunneling current is given:

$$J_{FN} = e\rho_n v_R \Theta \,, \tag{26}$$

with Θ the tunneling probability, and v_R the Richardson velocity:

$$v_R = \sqrt{\frac{k_B T}{2\pi m^*}} \,. \tag{27}$$

This is the average velocity of the electrons that approach the barrier.

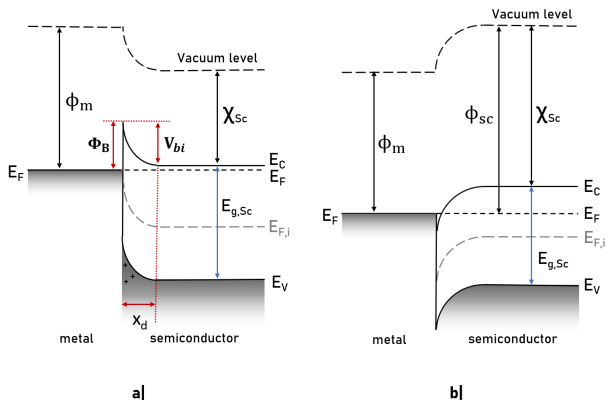


Fig. 13: The two types of band alignment that yield Ohmic contacts (for a n-type semiconductor):
a| A thin tunnel barrier created by a very high doping concentration.
b| Band alignment at zero bias for $\phi_m < \phi_{sc}$.

The tunneling probability Θ can be easily be derived from the time-independent Schrödinger equation in the WKB approximation for a slowly varying potential [67][68]:

$$\psi(x) = \psi(0)\exp\left[-\int_0^x \frac{\sqrt{2m^*[V(x')-E]}}{\hbar}dx'\right], \quad (28)$$

For a triangular barrier with a width δ:

$$V(x) - E = e\Phi_B^0(1 - x/\delta), \quad (29)$$

the tunneling probability can be expressed as:

$$\begin{aligned}\Theta &= \frac{\psi(\delta)\psi^*(\delta)}{\psi(0)\psi^*(0)} \\ &= \exp\left[-2\int_0^\delta \frac{\sqrt{2m^*}}{\hbar}\sqrt{e\Phi_B^0\left(1-\frac{x}{\delta}\right)}dx\right] \\ &= \exp\left[-\frac{4}{3}\frac{\sqrt{2m^* e\Phi_B^0}\delta}{\hbar}\right]\end{aligned} \quad (30)$$

The tunneling probability, and thus the tunnel current increasing for larger negative bias voltages, as this changes the aspect ratio of the triangular barrier. The tunneling current also increases with the doping concentration as this decreases the depletion region/tunnel barrier width. At doping concentrations than 10^{18}cm^{-3} field emission dominates the carrier transport (at small bias voltages). The tunneling current also increases with temperature. However, at high temperatures thermionic emission becomes the dominant transport process.

Thermionic emission: Thermionic emission is the emission of hot electrons into the vacuum, or in the case of a metal-semiconductor interface: into the empty conduction band of the semiconductor [59][65][69]. For low bias voltages the thermionic emission current is given by:

$$I_{TE} = A^{**}T^2\exp\left(-\frac{e\Phi_B^0}{k_BT}\right)\left[\exp\left(\frac{eV_{bias}}{k_BT}\right) - 1\right] \quad (31)$$

with A^{**} the product of the interface area and the effective Richardson constant A_R^* [70]. This model has been shown to be in good agreement for many material systems at non-cryogenic temperatures [71][72][73][74].

However, this model can be refined to include some interface effects. One important barrier lowering mechanism is the Schottky effect. Free charges in the semiconductor induce a surface charge at the metal interface to shield the bulk metal. The resulting electric field can be expressed in terms of mirror charges. In addition to the potential due to the mirror charge, the charge distribution in yhe depletion region contributes to the potential landscape for an electron in the conduction band of the semiconductor. For now the field due to the depletion region will be denoted by E_0. In sec.III-A the depletion region will be discussed in more detail. For an electron at a distance x from the interface, the potential due to the mirror charge and the depletion region can now be expressed as:

$$V(x) = \frac{e}{16\pi\epsilon_{sc}x} - E_0 x \quad (32)$$

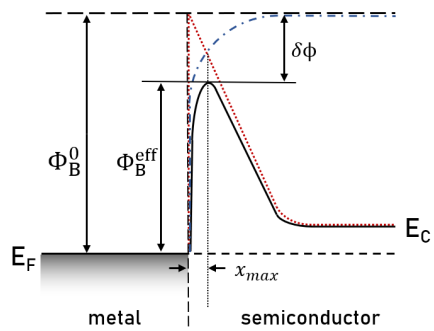


Fig. 14: Barrier lowering due to the Schottky effect. Sketched are the potentials due to the image charge (blue dash-dotted line), and due to the depletion region (red dotted line), both relative to the unperturbed barrier height Φ_B^0. The resulting barrier is sketched in black. Indicated are the barrier lowering $\delta\phi$ and the effective barrier height Φ_B^{eff}.

This potential will have a maximum at position x_{max}, close to the interface:

$$x_{max} = \sqrt{\frac{e}{16\pi\epsilon_{sc}E_0}}. \quad (33)$$

Substituting this back into eq.32 yields a lowering of the barrier:

$$\delta\phi = \sqrt{\frac{eE_0}{4\pi\epsilon_{sc}}} \quad (34)$$

The resulting barrier is sketched in fig.14. The effective Schottky barrier height can now be expressed as:

$$\Phi_B^{\text{eff}} = \Phi_B^0 - \delta\phi. \quad (35)$$

Note that the barrier lowering implicitly depends on the applied bias voltage through the band bending/depletion region width. This dependence can be quantified through the ideality factor n [60][70][75]:

$$n = \left(1 - \frac{\partial\Phi_B^{\text{eff}}}{\partial V_{bias}}\right)^{-1} \quad (36)$$

Using both the effective barrier height and the ideality factor, the thermionic emission current can be expressed as:

$$\begin{aligned}I_{TE} =& A^{**}T^2\exp\left(-\frac{e\Phi_B^{\text{eff}}}{k_BT}\right)\exp\left(\frac{eV_{bias}}{nk_BT}\right) \\ &\times\left[1 - \exp\left(-\frac{eV_{bias}}{k_BT}\right)\right]\end{aligned} \quad (37)$$

For $\Phi_B^{\text{eff}} = \Phi_B^0$ and $n = 1$, this reduces to eq.31.

A last remark: the Schottky barrier height is not necessarily constant over the interface. Surface roughness can result in local field enhancement, and therefore in stronger Schottky barrier lowering. The ideality factor n is the average barrier lowering due to a bias voltage, and therefore depends also implicitly on the surface roughness: the cleaner the interface, the lower the ideality factor will be [70].

C. Surface states and Fermi level pinning

Up until this point we have treated the contact formation between the metal and the semiconductor as a semiclassical electrostatic problem. This is useful for the description of macroscopic and mesoscopic phenomena, such as carrier transport. However, a microscopic description of the actual interface can illuminate the shortcomings of the Schottky-Mott model and describe the interface formation a lot more accurately. Several types of electronic states can form at the interface. The density of these surface states and their occupation determine the band alignment, and therefore the behaviour of the contact formation.

Intrinsic surface states arise from the broken translational symmetry at the surface. The wave function of an electron in a semi-infinite perfect crystal is invariant under translation with the period of of the crystal in both directions parallel to the interface. Therefore the investigation of the surface reduces to a one-dimensional problem. The potential in the direction perpendicular to the interface is given by:

$$V(x) = \begin{cases} V_c \cos\left(\frac{2\pi x}{a}\right) & x < 0 \\ V_0 & x > 0 \end{cases}, \tag{38}$$

which is periodic (with period a in the crystal and constant outside it, as is shown in fig.15a.
Now the Schrödinger equation can be solved for this potential. An electron in the crystal will back scatter elastically when it hits the surface. Therefore the general the wave function inside the crystal ψ_c can be expressed as a superposition of two counterpropagating waves with wave vectors $\kappa \pm \pi/a$:

$$\psi_c = Ae^{i(\kappa+\pi/a)x} + Be^{i(\kappa-\pi/a)x} \tag{39}$$

Outside the crystal the wave function decays exponentially:

$$\psi_0 = C\exp\left(-\sqrt{\frac{2m}{\hbar^2}(V_0 - E)}x\right) \tag{40}$$

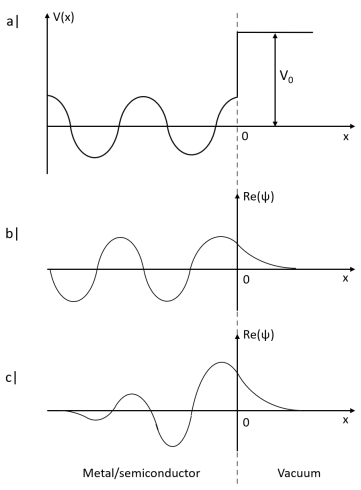


Fig. 15: A model for the interface of a crystalline conducting solid
a| Sketch of the semi-infinite Bloch potential that models the edge of the crystal.
b| The resulting Bloch wave that decays exponentially into the vacuum.
c| Solution to the Schrödinger equation for an imaginary k-vector: this allows for the formation of a surface resonance.

The general solution to the Schrödinger equation in all space requires that the values of the wave functions and their first derivatives to the relevant spatial coordinate match. This solution is sketched in fig.15b: it is just a Bloch wave that decays into the vacuum. The electronic energy levels of these states are slightly modified with respect to their bulk values

Additional solutions are possible if we allow for imaginary κ. The resulting wave functions decay in *both* directions, as is shown in fig.15c. These surface resonances are therefore confined within a few Ångstrom from the interface. One can also look at the termination of a crystal in the Linear Combination of Atomic Orbitals (LCAO) framework. Then these surface states correspond to the concept of dangling bonds. The problem described above, is treated in much more detail by e.g. Lüth [76].

Similar interface states are formed in the semiconductor band gap at a metal-semiconductor interface. The tails of the wavefunctions of the delocalised electrons in the metal decay into the semiconductor band gap: electronic states are formed in the band gap at the interface. These surface states are named Metal-Induced Gap States (MIGS), and they are an intrinsic consequence of the breaking of the translational symmetry perpendicular to the surface.
Next to these intrinsic surface states, also extrinsic surface states exist. These extrinsic states are electronic states that are charged/trap charges, which are caused by imperfections or defects on the interface [76][77].

Fig.16a and b show sketch of a part of the band gap of a narrow band gap semiconductor, and the resulting density of surface states N_{ss}. Indicated is the branch point energy E_n. The surface states below this energy behave as donors: they are neutral when they are occupied, and positively charged if this is not the case. The states above the branch point are acceptor-like.

The position of the Fermi level relative to relative to this branch point determines the sign and amount of net charge on the interface. This surface charge is the microscopic origin the band bending described by the Schottky-Mott rule, and thus determines the Schottky barrier height [57]. The barrier height and the surface density of states N_{ss} can be related through:

$$\begin{aligned} E_g - e\Psi_s - e\Phi_B = & \frac{1}{eN_{ss}\sqrt{2e\epsilon_{sc}N_{d/a}(\Phi_B - \phi_n)}} \\ & - \frac{\epsilon_i}{eN_{ss}\delta}(\phi_m - \chi_{sc} - \Phi_B) \end{aligned} \tag{41}$$

with the surface potential Ψ_s the difference between the intrinsic Fermi level at the interface and in the bulk (see sec.III-A). The interface is modelled in this expression as a very thin dielectric layer which is transparent for electron transport. This interface layer has a thickness δ ($O(\text{Å})$), and an effective dielectric constant ϵ_i.

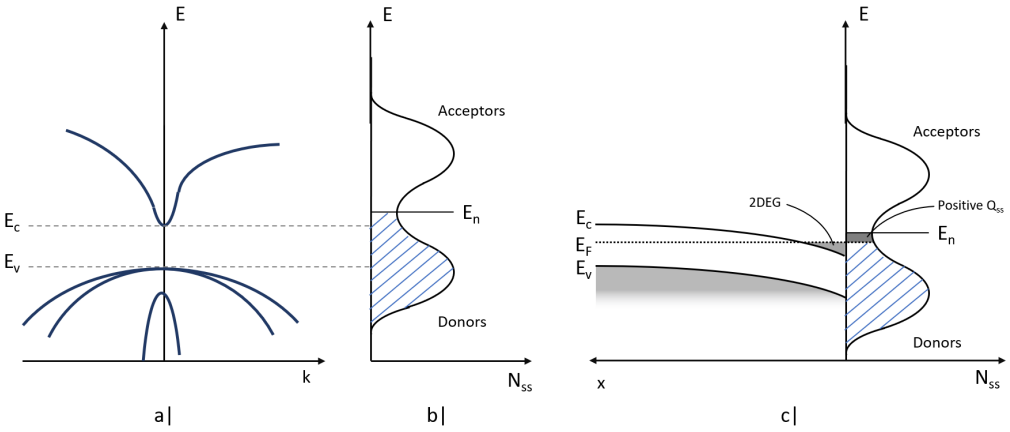


Fig. 16: Fermi level pinning in narrow band gap semiconductors
a| Sketch of the band gap of an arbitrary narrow band gap semiconductor.
b| Surface state density resulting from the dispersion in **a**.
c| Band bending caused by the positioning of the Fermi level in the surface DOS. A 2DEG is formed at the interface by pinning the Fermi level in the conduction band. The charges of the surface states and the 2DEG are equal in magnitude.

Two limiting cases for this model can be examined:

1) $N_{ss}\delta \to 0$: the interface layer disappears. In this case the expression above reduces to the familiar Schottky-Mott rule:
$$\Phi_B = \phi_m - \chi_{sc} \tag{42}$$
2) $N_{ss} \to \infty$: The surface charge density dominates the band bending. In this case the Fermi level gets pinned at in the band gap at the surface potential Ψ_s:
$$\Phi_B = \frac{1}{e}(E_g - e\Psi_s) \tag{43}$$

This Fermi level pinning is very important in the determination of the Schottky barrier height [76][78][79]. However, the surface density of states N_{ss} cannot easliy be determined, either experimentally or analytically.

Generally Fermi level pinning is a dominant effect in narrow band gap semiconductors, such as InAs and InSb [80]. Fig.16a and b show a sketch of a the band gap of such a semiconductor, and the resulting IFIGS density. Because of the position of the Fermi level in this surface DOS, the donor states between the Fermi level and the branching point are unoccupied; a positive surface charge exists, independent of any metal that ma be used for contact formation. The conduction band is then dragged below the Fermi level: a two-dimensional electron gas (2DEG) is formed at the interface to shield the semiconductor from the surface charge.
This has for example been verified for InAs: the Fermi level pinned into the conduction band by about 50meV [81][82].

Several groups have investigated Fermi level pinning and its influence on contact formation on PbTe, and report conflicting results. Lai and Cerrina et al. performed cyclotron photo-electron spectroscopy experiments to investigte metal-PbTe interfaces [83][84]. After cleaving PbTe crystals in UHV, several metals were deposited in-situ on the cleave (100) surface. They found generally no correlation between Φ_B^0 from expected from the Schottky-Mott rule and the experimental values. This indicates that surface charges play an important role. Interesting to note is that generally no atomically abrupt surfaces are formed during the metal deposition: several metals interdiffusion or even the formation of complexes with Te extracted from the substrate. This creates an extended interface layer whose barrier formation is difficult to predict. The exception was gold as a contacting metal: this formed an abrupt, nonreacted interface on the PbTe sample.
In contrast to these results: Walpole and Nill found some unpredictable band bending, but no Fermi level pinning on PbTe in their C-V and I-V electrical characterisation of several metal-PbTe interfaces [85].

III. Working principles of the nanowire MOSFET

In the most general terms, a transistor is a device where one terminal (the gate) controls the current that flows between two other terminals (the source and drain). One of the most common types of transistor is the Metal-Oxide-Semiconductor Field-Effect Transistor, or MOSFET.
Conventional MOSFET devices, as sketched in fig.17a, are fabricated on a doped semiconducting substrate. Using techniques like ion bombardment the doping density in the substrate can locally be changed to form metallic regions. These areas can be used as the source and drain contacts of the MOSFET. The area between the contacts then forms the channel. An insulating oxide layer with a third contact, the gate, are deposited on top of this channel. By applying a potential to the gate, the charge density can be modulated in the channel between the source and drain contacts.
The design of nanowire MOSFET flips the MOS stack upside down (see fig.17b). A degenerately doped (metallic) silicon substrate with a back contact is used as a gate. The thermal oxide functions as the insulating layer. Then a semiconducting nanowire is transferred on top, completing the MOS stack. Metallic leads are deposited directly on top of the semiconducting nanowire to form the source and drain contacts. Despite the inverted design, the working principles of both designs are identical.

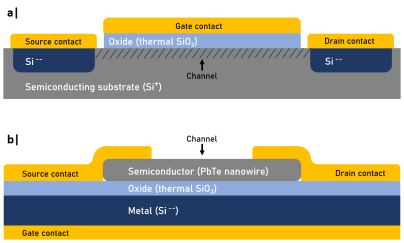


Fig. 17: Schematic cross-section of two MOSFET designs:
a| Conventional MOSFET: the source and drain contacts are formed by ion implantation in the semiconducting substrate. The substrate, an insulating oxide layer, and a metal gate contact form the MOS stack. The carrier density in the channel (shaded area in the substrate) can be influenced by applying a potential on the gate. The particular device sketched here is a n-channel enhancement mode MOSFET [59].
b| Nanowire MOSFET: The oxidised Si^{--} substrate with the PbTe nanowire on top together form the MOS stack. The addition of source and drain contacts on the nanowire, and a gate contact on the heavily doped substrate, completes the device architecture.

A. *MOS stack: gate behaviour*

For now let us ignore the source and drain contacts, and examine just the metal-oxide-semiconductor stack. Fig.18a shows the energy bands of the different layers of the MOS stack in isolation. Here, a heavily n-doped (metallic) semiconductor acts as the metal, as Si^{--} substrates are used in this project.
According to the Schottky-Mott model (see sec.II) the energy bands will deform close to an interface between different materials [59]. The Fermi levels in the metal and semiconductor will line up to satisfy electrostatic equilibrium; no spontaneous current will flow. In contrast to the metal-semiconductor interface discussed before, no charge exchange between the metal and semiconductor can take place due to the presence of the insulating oxide layer. This results in the formation of space-charge regions at the metal-oxide and oxide-semiconductor interfaces. The charge accumulation results in the bending of the bands:

- The charge density in the metallic layer is quite large, and will therefore be effectively screened from external charges or potentials. No space-charge region will be formed in the metal: charges will accumulate only at the metal-oxide interface.
- The absence of free carriers in the oxide will result in an electrostatic potential V_{ox} over the oxide layer.
- The smaller charge density in the semiconductor will result in the formation of a space-charge region at the oxide-semiconductor interface. This will be discussed in more detail below.

The band alignment for the layers in fig.18a is sketched in fig.18b.

For a further discussion of the band bending in the MOS stack, two important potentials need to be defined: the Fermi potential Ψ_F and the surface potential Ψ_s. Both are indicated in the band diagram in fig.18b.
The Fermi potential is defined as the difference between the intrinsic Fermi level $E_{F,i}$ and the actual Fermi level E_F in the bulk of the semiconductor, and can thus be regarded as a measure for the doping of the semiconductor:

$$e\Psi_F = E_{F,i} - E_F \tag{44}$$

$$= k_B T \exp\left[\frac{N_{d/a}}{n_i}\right] \tag{45}$$

Here $N_{d/a}$ is the donor/acceptor density, respectively.
The surface potential quantifies the band bending in the system. It is defined as the difference between the intrinsic Fermi level in the bulk and at the interface:

$$e\Psi_s = E_{F,i}(\text{surface}) - E_{F,i}(\text{bulk}) \tag{46}$$

Especially this surface potential plays a central role in the description of (the modification of) the band alignment.

The band bending, and therefore the accumulation of charge at the oxide-semiconductor interface, can be influenced by applying a potential over the MOS stack. The effect of this gate voltage V_g can be described by:

$$V_g = V_{ox} + \Psi_s + \phi_{ms} \tag{47}$$

The work function difference between the metal (Si^{--}) and semiconductor ϕ_{ms} is completely defined by the semiconductor band gap ($E_{g,sc}$) and doping, and the electron affinities of both materials ($\chi_{Si^{--}}, \chi_{sc}$):

$$\phi_{ms} = \chi_{Si^{--}} - \left[\chi_{sc} + \frac{E_{g,sc}}{2e} + \Psi_F\right] \tag{48}$$

This expression is independent of the applied voltage. Therefore the oxide and surface potentials, and thus the band bending, are directly influenced by the gate.
An important value of the gate voltage is the flat-band voltage. This is the gate potential needed to counteract the band bending caused by the Fermi level alignment:

$$\Psi_s = V_{ox} = 0\,. \tag{49}$$

In this case no space-charge regions are present in the entire MOS stack.

Consider now a p-type semiconductor with ideal band alignment ($V_{FB} = 0$). This means that the flat-band condition is satisfied if no gate potential is applied. This is shown schematically in fig.18c. Based on this idealised system we will discuss how the gate can tune the charge density in the semiconductor. For other material systems ($V_{FB} \neq 0$) the exact same reasoning is correct, but with respect to $V_g = V_{FB}$ instead of $V_g = 0$.
If a negative voltage is applied on the gate with respect to the (p-type) semiconductor, holes will accumulate at the oxide-semiconductor interface. This *accumulation layer* of majority carriers shields the bulk of the semiconductor from the applied voltage. The resulting gradient in carrier concentration at the interface leads to band bending at the interface, see fig.18d.
In the opposite case, the positive voltage on the gate will repel the holes from the oxide-semiconductor interface. This creates a negative space-charge region due to the fixed ionised acceptor atoms. Here this so-called *depletion region* screens the bulk semiconductor, which results in upward band bending. This is shown in fig.fig.18e.

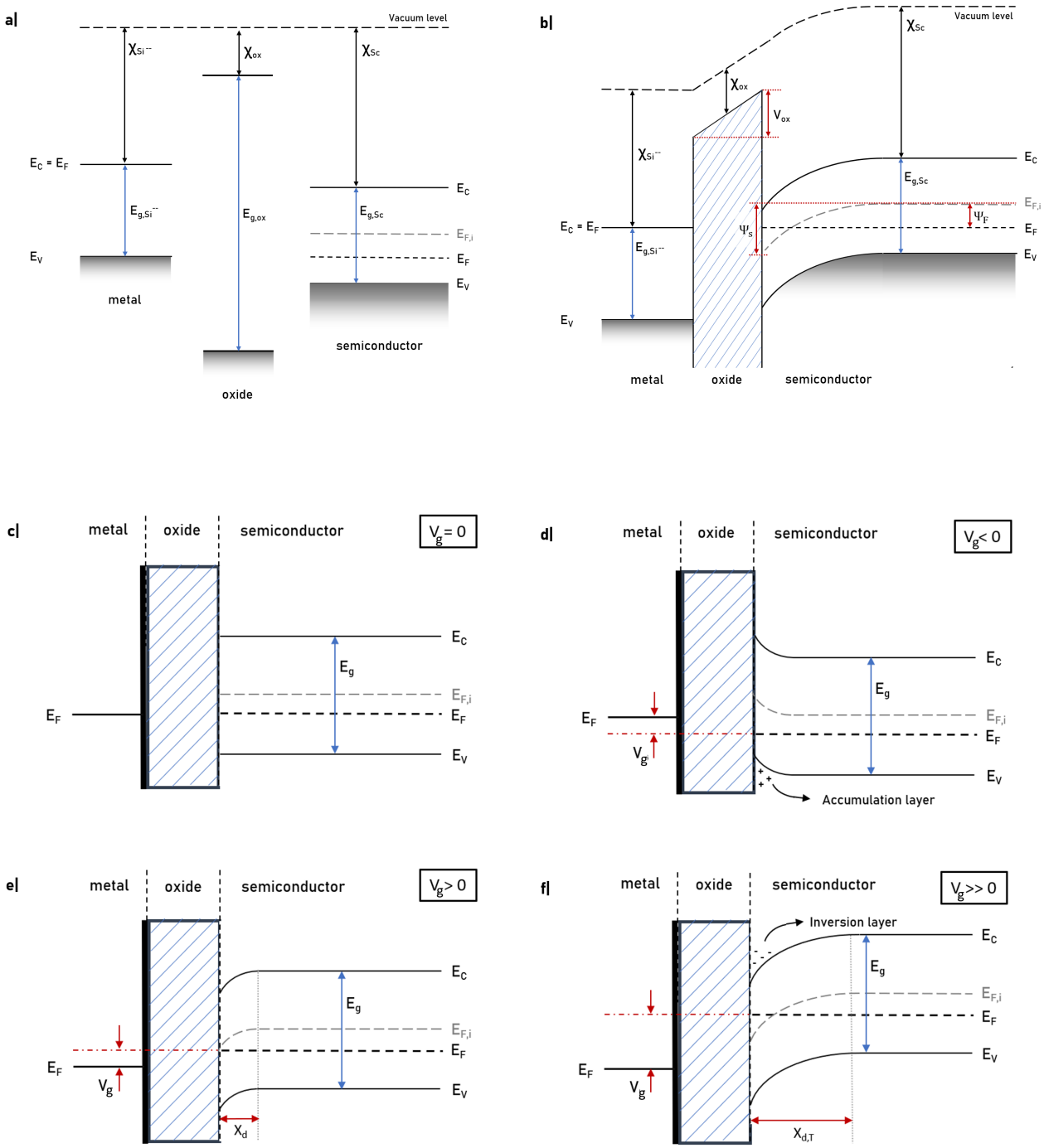


Fig. 18: Energy band alignment of a metal-oxide-semiconductor stack for a p-type semiconductor.
a| The energy bands of degenerately doped (metallic) silicon, an oxide, and a p-type semiconductor in isolation. All energy bands are aligned to the vacuum level. Indicated are the band gaps (E_g) and electron affinities (χ) of the three materials.
b| Deformation of the energy bands due to alignment of of the Fermi levels. Again the band gaps and electron affinities are indicates, as well as the Fermi potential and the surface potential.
c-f| The influence of an applied gate voltage on the energy bands. An idealised MOS stack ($V_{FB} = 0$) is shown to show the influence of the gate potential independently of the band alignment as discussed above. Fig.**c** shows the band alignment of this simplified system without an applied voltage. For other material systems this is equivalent to $V_g = V_{FB}$. If a negative gate voltage is applied (compared to V_{FB}), the energy bands bend downwards to lower energies. An accumulation layer is formed at the interface (fig.**d**). If a positive voltage is applied to the gate (fig.**e**), the bands bend upwards; a depletion layer with with x_d is formed. For large negative gate voltages the intrinsic and actual Fermi levels cross (fig.**f**); an inversion layer is formed at the interface.

The width of the depletion region x_d can be derived from Poisson's equation [86]:

$$\frac{dE}{dx} = \frac{\rho(x)}{\epsilon_{sc}}\,, \tag{50}$$

with ϵ_{sc} the permittivity of the semiconductor.
In this region the charge density $\rho(x)$ is determined by dopant concentration $N_{d/a}$, which is assumed to be uniform:

$$\rho(x) = \pm e N_{d/a}\,, \tag{51}$$

with the plus (minus) sign for donor (acceptor) dopants, respectively. Substituting this in eq:50, and integrating with the boundary condition $E(x_d) = 0$ yields:

$$E(x) = \mp \frac{eN_{d/a}}{\epsilon_{sc}}(x - x_d) \tag{52}$$

Using $E = -\boldsymbol{\nabla} \cdot V$ and integrating over x again yields:

$$V(x) = \pm \frac{eN_{d/a}}{2\epsilon_{sc}}(x - x_d)^2 \tag{53}$$

Now this can be combined with the surface potential $\Psi_s = V(x = 0) - V(x_d)$, where $x = 0$ i defined to be at the interface. Rewriting then yields an expression for the depletion region width:

$$x_d = \left(\frac{2\epsilon_{sc}\Psi_s}{eN_{d/a}}\right)^{1/2}. \tag{54}$$

For large positive voltages, the intrinsic Fermi level at the surface moves below the Fermi level: the semiconductor locally becomes n-type. An *inversion layer* of electrons is formed at the interface. At a certain gate voltage, the surface potential is twice as large as the Fermi potential:

$$e\Psi_s = 2\Psi_F \tag{55}$$

If this condition is satisfied, the inversion charge density is equal to the bulk carrier concentration: bulk is completely shielded. This means that the depletion region width is constant [60]. Equation 55 can the be expressed as:

$$x_{d,T} = \left(\frac{4\epsilon_{sc}\Psi_F}{eN_{d/a}}\right)^{1/2} \tag{56}$$

From this point onward the inversion charge density increases exponentially with the surface potential. The surface charge region at the interface (which acts as the channel of the transistor, see sec.III-B), behaves as a n-type semiconductor.The point where the doping behaviour inverts is called the threshold inversion point, and equation 55 is the threshold inversion condition.
The applied gate voltage to needed to achieve this condition is called the threshold voltage [59]:

$$V_{Th,i} = \frac{eN_{d/a}x_{d,T}}{C_{ox}} + V_{FB} + 2\Psi_F \tag{57}$$

This expression can be found by plugging the flat-band condition (eq.49) and the threshold inversion condition (eq.55) in the expression for the gate voltage in eq.47. The first term describes the potential between the gate and the depletion layer. The oxide capacitance C_{ox} will discussed in sec.C in detail.

From this expression it becomes clear that the threshold condition depends on the doping density, oxide capacitance, and the material choice/band alignment.

The charge density in the semiconductor as a function of the surface potential Ψ_s for the different regimes discussed above, are sketched in fig.19.
For an n-type semiconductor, the behaviour as discussed before is exactly inverted: the majority and minority carriers switch roles, and the accumulation, depletion, and inversion regimes occur for gate potentials of the opposite sign.

So here we have established that the gate potential can tune the carrier density and type in the semiconductor close to the oxide-semiconductor interface. In a regular MOSFET, it is exactly this region that forms the channel between the source and drain contacts. So the gate can control the channel conductance.
In a nanowire MOSFET the diameter of the wire limits the width of the channel. So if the depletion width x_d is larger than the nanowire diameter, the gate can tune the carrier density and type in the entire wire

B. Ideal nanowire MOSFET operation and extraction of transport properties

Let us now examine the MOSFET structure in its entirety by adding Ohmic contacts on both ends of the semiconductor material (fig.20a). The current through the channel obeys Ohm's law:

$$I_d = GV_{sd}\,, \tag{58}$$

With I_d the drain current,G the channel conductance and V_{sd} the source drain voltage.

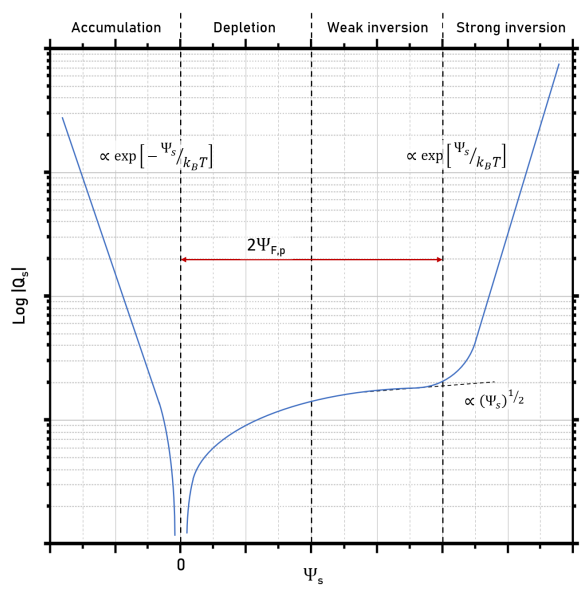


Fig. 19: Absolute value of the charge density at the oxide-semiconductor interface plotted as a function of the surface potential. Indicated are the different regimes. Based on [60]

To derive an expression for the channel conductance, we will express the drain current based on eq.18 as:

$$I_d = \int e\rho_{n/p} v_d \, dA \tag{59}$$

Using equations 20 and 23 and integrating the charge density over the cross-sectional area A of the nanowire, this can be rewritten as:

$$I_d = \frac{\mu_{e/h} Q V_{sd}}{L^2} \tag{60}$$

with Q the total charge in the nanowire, and L the channel length. The charge can then be expressed in terms of the capacitive coupling to the gate:

$$Q = C_{ox}(V_g - V_{FB}) \, , \tag{61}$$

with V_{FB} the flat band gate voltage. In literature this voltage is also often referred to as the pinch-off voltage the (accumulation) threshold voltage $V_{th,a}$, which should not be confused with the inversion threshold voltage discussed before [57][59][65]. The accumulation threshold voltage is the division between the accumulation and depletion regimes. Therefore it indicates the presence of majority carriers in the system, whereas the inversion threshold signifies the introduction of free minority carriers into the system.
Eq.61 also introduces the capacitance of the oxide layer C_{ox}. The capacitances in the system and their influence on the extraction of transport properties will be discussed later in sec.III-C.

By substituting eq.61 in eq.60 the drain current can be rewritten as:

$$I_d = \frac{\mu_{n/p} C_{ox}}{L^2}(V_g - V_{th,a})V_{sd} \tag{62}$$

This way the drain current is expressed just in terms of material properties ($\mu_{n/p}$, C_{ox}, $V_{Th,a}$) and geometry (C_{ox}, L) of the particular device, and the applied voltages (V_g, V_{sd}). In the same vein, the channel conductance can be denoted as:

$$G(V_g) = \frac{\mu_{n/p} C_{ox}}{L^2}(V_g - V_{th,a}) \tag{63}$$

In practice, this is rarely what is measured: for increasing gate voltages the contribution of other resistances in the system limits the conductance. This can be modelled by adding a series resistance R_s to eq.63 [87][28]):

$$G(V_g) = \left(R_s + \frac{L^2}{\mu_{n/p} C_{ox}(V_g - V_{th,a})} \right)^{-1} \tag{64}$$

This series resistance includes all other resistances in the system, such as the line resistance of the metallic contacts and the interface resistance. This model is fitted against the actual measured conductance trace of a InSb nanowire MOSFET device in fig.20b [87].

The dependence of the drain current on the gate voltage is called the transconductance:

$$g_m = \frac{dI_d}{dV_g} \tag{65}$$

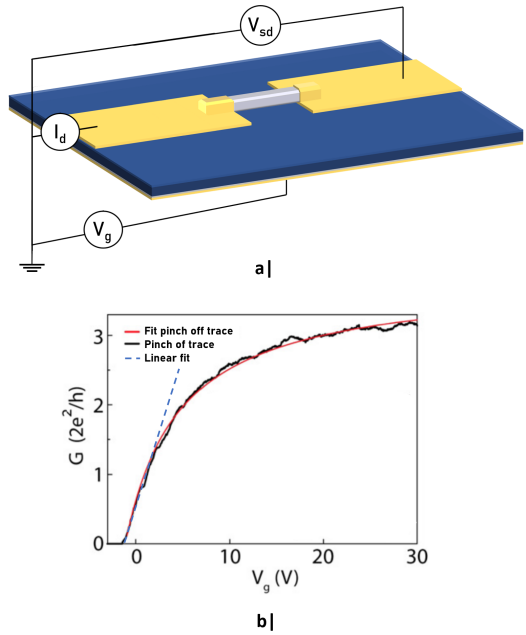


Fig. 20: Electronic transport measurements on a nanowire MOSFET. **a**| Schematic depiction and wiring scheme of a nanowire MOSFET. **b**| Experimental $G(V_g)$ trace at constant V_{sd} (black) of a InSb nanowire MOSFET with a linear fit (blue) for low V_g and a fit including a series resistance (red). Adapted from O. Gül et al.[87].

According to eq.63 the transconductance can be determined from a linear fit for low V_g through the measured $I_d(V_g)$ or $G(V_g)$ traces. This is indicated with the blue dotted line in fig.20b. In this manner the carrier mobility in the device can be determined using:

$$\mu_{n/p} = \frac{g_m L^2}{C_{ox} V_{sd}} \, . \tag{66}$$

From this fit also the pinch-off voltage $V_{th,a}$ can be determined, which in turn can be used to determine the carrier density in the wire[51]:

$$\rho_{n/p} = \frac{C_{ox} V_{th,a}}{e \, d^2 L} \, , \tag{67}$$

where d is the diameter of the nanowire. Here it is assumed that the wire has a square cross-section.

C. Capacitance

The capacitance is an important property of the MOSFET device, as it is used in the extraction of both the carrier mobility (eq.66) and density (eq.67). To calculate the capacitance, a back-gated nanowire is commonly modelled as a metallic cylinder with radius R, whose center is separated from an infinite metal plate by a distance t (see fig.21a). This idealised model yields the following analytical expression for the capacitance C_{ox}[88][89]:

$$C_{ox} = L \frac{2\pi\epsilon_0\epsilon_r}{cosh^{-1}(t/R)} \tag{68}$$

However, there are some significant differences between this model and the actual physical system of a back-gated semiconductor nanowire. This model assumes that the entire half-space above the infinite metal is filled with one and the same dielectric material. In reality the wire is not

completely embedded: it lies on top of a the oxide layer of the MOS stack, and all other sides are exposed to a vacuum. The smaller dielectric constant of the vacuum results in weaker confinement of the electric field. To illustrate this the equipotential lines are plotted in fig.21b.
Finite element simulations performed by Wunnicke [88] have shown that this difference can be accounted for by introducing an effective dieectric constant. The relative dielectric constant for SiO_2 often cited in literature is $\epsilon_r = 3.9$ [90]. Wunnicke shows that an effective dielectric constant of $\epsilon_{r,eff} = 2.2$ acurately models the actual geometry within an error margin of 3% for a large range of geometries [88]. The introduction of such an effective dielectric constant only works because the difference between the dielectric constants of SiO_2 and the vacuum is relatively small.

Moreover, PbTe nanowires are not circular, but approximately square in diameter. Wunnicke also modelled the effect of the cross-sectional geometry of the nanowire on the capacitance (see fig.21c). He proposed that this effect can be accounted for by introducing two modifications to the metallic cylinder-infinite plate model: a correction to the effective dielectric constant introduced in the previous point compensates for the changes to the electrostatics of the system. The effective dielectric constant for SiO_2 the becomes: $\epsilon_{r,eff} = 2.45$. The difference in cross-sectional area between a rectangular and a cylindrical wire can be negated by modelling the square cross-section as a circle with a larger effective radius $R^* = d/\sqrt{\pi}$.

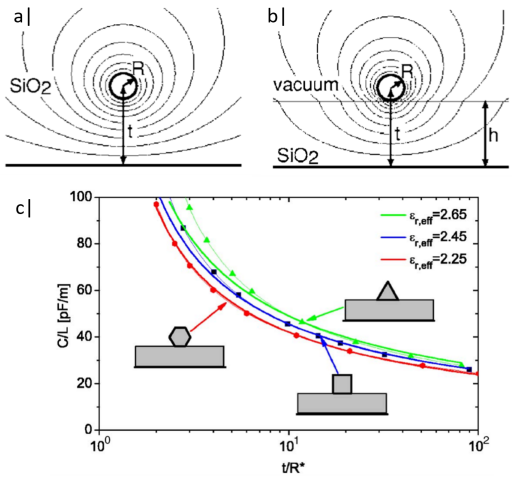


Fig. 21: Capacitive coupling between a metallic nanowire and an infinite metallic back gate:
a| Cross-sectional geometry of a metallic nanowire of radius R suspended in a dielectric (SiO_2) a distance t above an infinite metallic back gate. Also plotted are the corresponding equipotential lines.
b| Modification to the model sketched in **a**: the wire is positioned on a layer of gate dielectric of thickness h. The wire is exposed on all other sides to the vacuum. Plotted are again the equipotential lines. The differences between **a** and **b** are due to the difference in dielectric constant between the SiO_2 and the vacuum, leadin to stronger confinement of the electric field in **a**.
c| The effect of the cross-sectional geometry of the wire on the capacitance for a large range of device geometries. Plotted is the model compensated capacitance model (eq.69) against the capacitances calculated using finite element methods.
Adapted from Wunnicke [88].

The expression for the capacitance according to Wunnicke then becomes [88]:

$$C_{ox} = L\frac{2\pi\epsilon_0\epsilon_{r,eff}}{cosh^{-1}(\sqrt{\pi}t/d)} \tag{69}$$

Also, the wires are not metallic, but semiconducting. The lower carrier density results in further penetration of the field lines into the wire [89]. This results in a completely different gate response. However, semiconducting nanowire with a charge density higher than 10^{17}cm^{-3} behaves similar to a metallic wire [91][89]. Some initial measurements performed in the Frolov group at the University of Pittsburgh on PbTe wires grown in Eindhoven have shown carrier densities of this order of magnitude. Therefore this is concern is ignored for the rest of this thesis.

Also edge effects, most notably the presence of electrodes source and drain contacts, can screen the gate coupling. Generally: the shorter the channel length, and the wider/thicker the contacts, the stronger the screening effect [89][92][93]. Due to this electrostatic screening, the model described above will overestimate the capacitive coupling and therefore underestimate the mobility.

For future measurements at cryogenic temperatures also the effects of quantum confinement on the capacitance should be taken into consideration. Papers from the Kouwenhoven group in Delft usually assume a 20% reduction in the capacitance due to confinement effects [25][87]. To confirm this, the 3D Schrödinger-Poisson equation should be solved numerically for the material system and specific device geometry used.

Eventually for proper analysis of the transport properties of the nanowire MOSFET devices, the capacitance of the entire device has to be determined more precisely. This can either be done by modelling the entire device, including the charge distribution in the semiconductor, the effects of confinement (at low temperature), and edge effects/screening by the contacts. Or by directly measuring the capacitance. However, this poses its own challenges, as the capacitances involved are typically very small.

Device fabrication

In the previous chapter the working principles of nanowire MOSFET devices have been explained. Here the practical matters of the architecture and fabrication of (a chip of) such devices will be discussed. The goal here is to briefly explain the fabrication process step-by-step, as it will be of importance for the discussion of some of the results presented in chapter 6. A more detailed description can be found in appendix I.

I. Device architecture

The nanowire MOSFET devices are fabricated on 1×1 cm pieces of a diced, heavily n-doped silicon wafer with 100 nm of thermal oxide on both sides. The standard design used fits up to 36 devices onto one chip. A schematic depiction of a device chip is shown in fig.22.
One chip fits the relatively large number 36 similar devices because a significant fraction of the devices breaks either already during the fabrication procedure, or during (cooling down for) the transport measurements. By fabricating a chip with this many devices, still enough devices will survive to reliably draw conclusions from the measurement data.

Part of the metal-oxide-semiconductor stack as discussed in section 3.X can be recognised in the cross-section of the substrate used. The silicon is n-doped so heavily that the Fermi level is shifted into the conduction band; therefore it shows metallic behaviour. The metallic silicon and the thermal oxide (SiO_2) form the metal-oxide part of the MOS stack. Later in the fabrication process semiconductor nanowires will be deposited on top of the substrate, completing the stack. However, the bottom SiO_2 layer insulates the metallic silicon, thus preventing it from being used as a gate for the devices to be fabricated on top of the substrate. Therefore the bottom oxide layer is removed using reactive ion etching (RIE); a gold contact is deposited in its place. Thus a *global back gate* for all devices on the chip is created.
The devices on top of these substrates have to be designed with the probe station (measurement setup: see chapter 5) in mind. This measurement device has two movable arms that end in six fingers each. These arms can be used to contact the nanowire MOSFETs on the chip. Therefore "*cells*" of two rows of six gold contacts are deposited on top of the substrate. The spacing between these *contacts pads* corresponds to the fingers of the probe arms. The CAD design of one of these cells is shown in fig.23a. The light red shaded shapes are the contact pads.
In between these two rows of contact pads in a cell a field of golden *markers* can be found (blue in fig.23a). After the deposition of the contact pads and markers, the nanowires are transferred onto the marker field using the tissue transfer method with cleanroom tissue paper (also known as "swiping"). This method distributes the wires randomly over swiped area. Using a scanning electron microscope (SEM) the position of the wires on the marker field can be determined. Once the positions of the wires are known, an overlay CAD design can be made the connections between the ends of the wires and the contact pads: the *approach contacts*. These connections can now act as the source and drain contacts of the nanowire MOSFETS.

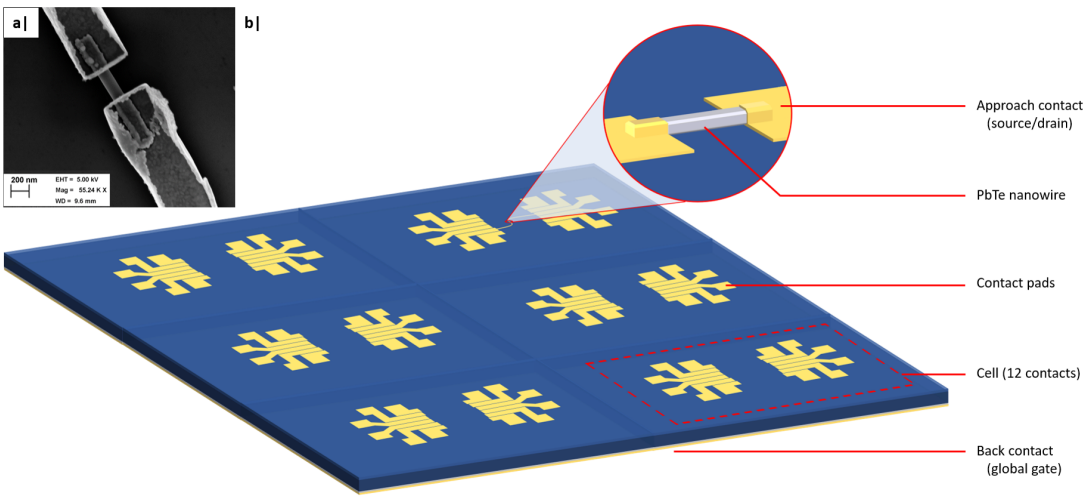


Fig. 22: Overview of the design of a chip with (up to) 36 nanowire MOSFET devices.
a| Top view SEM image of a nanowire MOSFET device. It shows the nanowire with its Ti/Au source and drain contacts.
b| A schematic drawing of a device chip with nanowire MOSFETs. Indicated are the global back gate, contact pads, and a cell consisting of 12 of these contacts. The magnification shows a nanowire with its source and drain contacts.

As has been discussed in Chapter 2, a native oxide forms on the PbTe nanowires as soon as they are exposed to air. If the (Ti/Au) approach contacts were to be deposited onto the wires directly, this oxide layer would act as a tunnel barrier for charge barriers during the transport measurements (see chapter 6 for experimental results that corroborate this). Therefore in situ argon ion milling is used to remove the native oxide before the deposition of the approach contacts. In principle the chip would now be completed. However, it was observed that just argon ion milling did not entirely remove the native oxide, regardless of the milling time (again see chapter 6). Therefore a short oxygen plasma etch was added before the argon milling step. Traces of organic material such as residue of the resist used (PMMA) can inhibit the argon ion milling. The oxygen plasma etch will remove these residues, but should not damage the nanowires.

II. Fabrication recipe

Here the fabrication recipe will be discussed step-by-step in a little more detail. The fabrication steps are numbered using Roman numerals in the recipe below. These numerals correspond to the ones indicated in fig.23b.

Back contact

I. The oxide on one of the two sides of the SiO_2-Si^{--}-SiO_2 substrate is removed using a CF_3H:O_2 plasma etch.

II. A 2 nm titanium adhesion layer and a 100 nm gold film are consecutively deposited on the cleared Si^{--} side of the sample by e-beam evaporation.

Contact pads and markers

III. The top side of the sample is spin-coated in PMMA. Using E-beam lithography (EBL) the design of the contact pads and marker fields are patterned into this resist layer. Then the resist is developed for 80s in MIBK:IPA. This leaves the substrate bare where the the PMMA was patterned, but leaves the resist intact everywhere else.

IV. Again a 2 nm Ti adhesion layer and a 100 nm Au layer are deposited via e-beam evaporation.

V. By leaving the sample in acetone for several hours the PMMA is dissolved, lifting off the excess metal in the process. Only the contact pads and the marker fields will be left behind.

Wire transfer

VI. Nanowires are transferred from the growth substrate to the marker fields by the tissue transfer method: the tip of a piece of cleanroom tissue paper is swiped over the growth substrate. Wires will break off and stick to the tip of the paper. Then by swiping the tip over the marker fields, some wires will inevitably detach from the tip and remain on the sample.
These wires can now be located using a SEM. Based on these SEM images, a design for the approach contacts as is depicted in fig.23a (bright red lines) can be created.

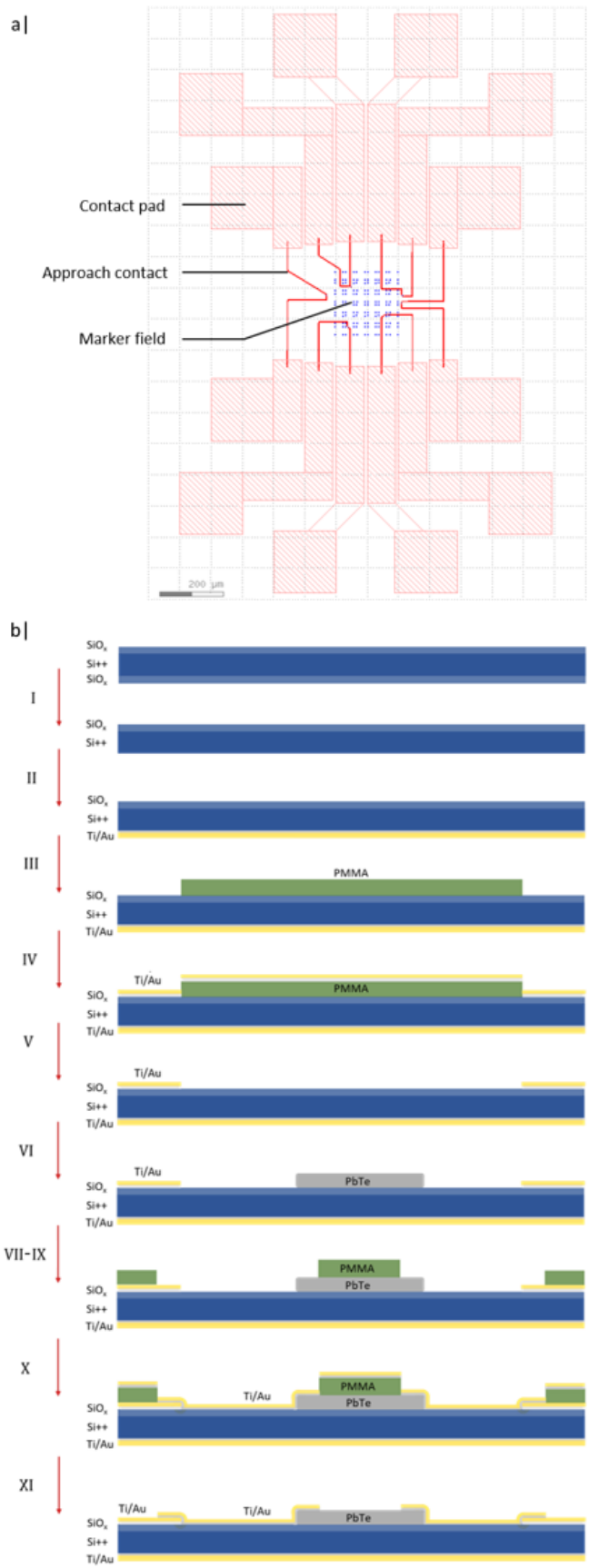


Fig. 23: Design (a) and fabrication procedure (b) of a nanowire MOSFET device chip. **a|** CAD design of one cell of a device chip. Indicated are the contact pads (shaded red), marker field (blue), and the approach contacts (bright red lines). **b|** Schematic overview of the fabrication procedure of the nanowire MOSFETs. A detailed explanation of each step can be found at the corresponding Roman numeral in section II.

Approach contacts

VII. The substrate is again spin-coated in PMMA. In a second EBL exposure the design of the approach contacts will be patterned into the resist. A perfect alignment of the substrate with the existing features to the design of the overlay exposure is key here. After the exposure, the resist is developed in the same way as described at number III.

VIII. To ensure that all resist is removed from the sample at the patterned areas, the sample is exposed to a 30s oxygen plasma etch[1]. Residual PMMA can inhibit the argon ion milling step. This can be prevented by performing this etching step.

IX. The native oxide is removed from the nanowires to ensure the formation of Ohmic contacts. Argon gas is blow out of a gun, ionised, and accelerated towards the sample. Upon impact the argon ions mill away material from the nanowire surface of the target. The rest of the sample is protected from the ion bombardment by the PMMA film.

X. The approach contacts are deposited by sputtering 20 nm titanium and 20 nm gold on the sample. The Ti should ensure good sticking of the contact to the wires and the substrate, and 20 nm Au should protect the titanium from oxidation. Afterward a 100 nm Au film is e-beam evaporated on top. This is done because e-beam evaporation has a much faster deposition rate and is more directional than sputtering. Especially the better directionality limits sidewall deposition and thus yields better contacts.

XI. In a final lift-off step in acetone, the PMMA film and the metal on top is removed, leaving the approach contacts behind.

[1] This step is not included in the fabrication procedure of all samples, see chapter 6. It will be explicitly indicated when it is omitted.

Electronic transport measurements

Transport measurements have been performed on the nanowire MOSFET devices to characterise the electronic properties of the nanowires. Here the measurement set up and procedure will briefly be explained.

The transport measurements were performed in a Janis ST-500 probe station. Fig.24a show a top-view photo of this set up, once it is opened up. All relevant component parts are indicated.
The vacuum vessel is pumped down to $10^{-}6$mbar using a turbomolecular pump. The sample chuck can be cooled down with liquid helium. Inside this sample chuck are also a thermocouple and a heating element. Using these in addition to the liquid helium flow allows for control of the temperature of the sample chuck in the range from 4.2K to 420K with an accuracy of 0.1K.

The device chip is placed on the electrically conducting sample chuck. Good electrical contact between the sample chuck and the global back gate is ensured by a droplet of conductive silver paint. Two movable probe arms protrude into the vacuum chamber; both end in six conductive tips. These arms can be placed on top of the contact pads on the device chip (see fig.24b. An optical microscope is used to control the placement of these probes.

A Keithley 4200 Semiconductor Characterization System is connected via three SMUs[1]to the probe arms and the sample chuck. A switch board determines to which of the probe tips it is connected. This Keithley can be used to apply a source-drain voltage and/or a gate voltage to a nanowire device, and measures the drain current. For a schematic depiction of the wiring, see fig.24c.

Using this set up two types of measurements can be performed.

- **I-V curves:** Current-voltage characteristics are measured by sweeping the source-drain voltage V_{SD} and measuring the drain current I_d. From the shape of these curves, the Ohmic or Schottky character of the contacts can be determined (see chapter 3). If the contact is Ohmic, the conductance of the device can be determined from the inverse slope of the I-V curve. A limitation here is the resistance of the measurement set up itself: in two-point measurements, the line resistance and internal impedance of the Keithley are part of the measured resistance. However, these can be measured a calibration measurement, and then subtracted from the total measured resistance to get the device resistance.

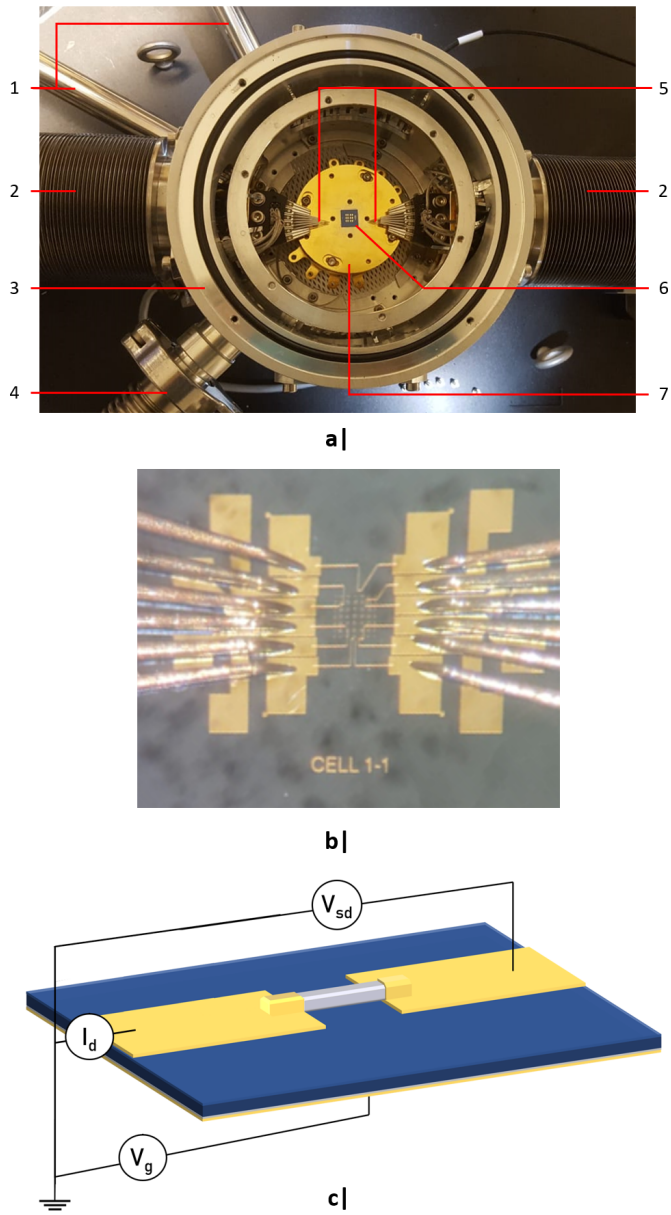


Fig. 24: Janis ST-500 probe station:
a| Top-view photo of the probe station when it is opened up. All relevant parts are indicated and numbered:

1	Helium lines (in/out)	5	Probe tips
2	Movable probe arms	6	Device chip
3	Vacuum vessel	7	Sample chuck
4	Line to turbo pump		

b| Close-up image of one cell on the device chip. Here the probe tips are landed on the contact pads, thus making a connection between the measurement set up and the chip.
c| Schematic depiction of one device. Schematically indicated is the wiring used for the transport measurements.

[1] A source measure unit (SMU) is a device that can both apply and measure a voltage and/or current.

- **Gate sweeps:** The gate dependence of the channel conductance (the transconductance g_m) can be determined from gate sweep measurement. In these measurements the drain current I_d is measured while sweeping the gate voltage V_g at a constant source-drain voltage. From these curves the doping character and density can be determined.

Unfortunately usually only up to a third of the devices on a chip provide useful data. Some of the device do not work due to issues during the fabrication process, for example due to leftover resist or a misalignment during one of the processing steps. However devices can also break during the measurements.

One issue that was observed quite often, was that devices stopped working after cooling the sample down to 10K. We suspect that this is due to the difference in thermal expansion coefficient between the contact metals (Ti/Au) and the nanowire. Therefore the contact between the metal and the wire can be broken when cooling down the sample.
Another issue is that the devices can ”blow up” when a high current flows through the wire. To protect the wire from this issue, a maximum allowed current (compliance) is set in the Keithley.
However, breakdown of the oxide can occur at high gate voltages. Then a sudden high current spike will flow between the gate and the wire/drain contact. Because the gate voltage is two to 4 orders of magnitude larger than the bias voltage, this breakdown current spike will destroy the wire.

Experimental results

Here the results of electronic transport measurements on the PbTe nanowire MOSFET devices are presented. First the contact formation will be studied, followed by an examination of the transport properties for nanowires of varying IV/VI ratios.
As the extensive treatise of the nature and behaviour of Schottky barriers in chapter 3 may have foreshadowed: it has been challenging to form Ohmic contacts on the PbTe nanowires. The contacts have been characterised, and a hypothesis that could explain the formation of the Schottky barriers is proposed.
These Schottky contacts prevent the accurate extraction of the mobility and carrier density from the $I(V_g)$ characteristics. However, the $I(V_g)$ curves do still give some qualitative information on the doping character as a function of the IV/VI ratio.

I. Ti/Au contacts on PbTe nanowires

For the analysis of the electronic transport properties of the PbTe nanowires, nanowire MOSFETs are fabricated (see chapter 4). The source and drain contacts are formed by sputter-deposited gold with a thin titanium adhesion layer. A top-view SEM image of such a device is shown in fig.25.
Several other groups have reported that the native oxide layer on the PbTe poses one of the biggest challenges for the formation of Ohmic contacts [51][94]. Lead oxides are wide band gap semiconductors [23]. A thin oxide layer will therefore create a tunnel barrier between the PbTe and the contact metal. This barrier behaves like a high Schottky barrier.
The formation of this native oxide starts the instant the MBE grown PbTe nanowires are exposed to air [51]. The TEM images in chapter 2 show that our PbTe nanowires end up up with a native oxide layer with a thickness of several nanometers.
Detailed XPS studies performed by Wang et al. [94], have shown that the Pb-O:Te-O bond ratio on crystalline films is approximately 8:1. The lead oxide will thus dominate the behaviour of the interface. The formed $(PbO)^{2+}$ complexes are electron traps, and will thus increase the density of surface states. The resulting band bending can explain the p-type conductivity that is often observed in oxidised undoped PbTe samples [94].

The first step in the fabrication of Ohmic contacts on PbTe should therefore be the removal of this oxide. The recipe developed in this project first asks for a short oxygen plasma etch to remove any residual (PMMA) resist. This is needed because some residual resist may inhibit the succeeding argon ion milling step. This argon ion milling is needed to actually etch away the native oxide.
Both etching processes have been systematically optimised to improve the the contact formation. The behaviour of the resulting contacts was investigated through electronic transport measurements at 10K. The results of the final step in this optimisation process is shown in fig.26.
Four chips with devices were made using nanowires from one and the same growth chip. In earlier tests it was found that an oxygen plasma etch of 30s was more than adequate to remove any residual PMMA resist from the nanowires.

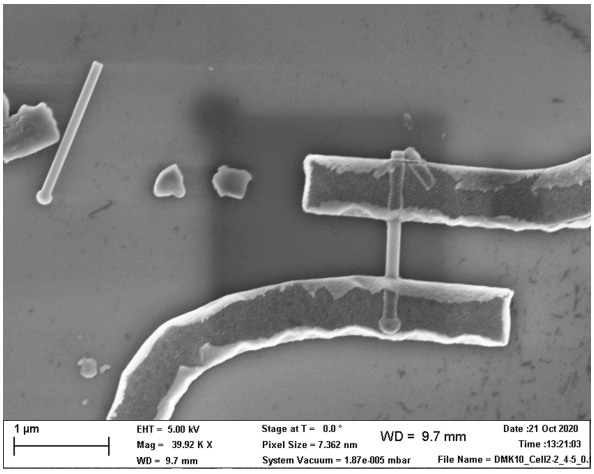


Fig. 25: Scanning electron microscopy (top-view) image of a PbTe nanowire MOSFET device with Ti/Au contacts. On the top left an uncontacted nanowire can be seen. On both the contacted and uncontacted nanowires the catalytic gold particle is clearly visible.

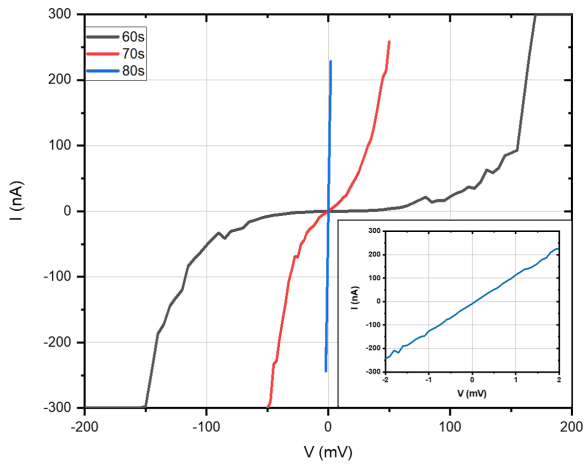


Fig. 26: $I(V_{sd})$ traces at T=10K of the Ar milling optimisation series. Shown are the curves measured on devices after 60s (black), 70s (red), and 80s (blue) of Ar milling. The shorter milling times still show Schottky-like behaviour, indicating that the native oxide is not yet fully removed. The blue curve, corresponding to 80s of Ar milling, appears to be just a vertical line when plotted at the same scale as the other curves. This data is replotted on a more suitable scale in the inset at the right bottom corner. Here one can clearly see the linear behaviour corresponding to an Ohmic contact.

To optimise the consecutive Ar milling step, each sample was etched for a different duration (60s, 70s, 80s, or 90s). Directly afterwards the source and drain contacts (5nm Ti/100nm Au) were in-situ sputter-deposited.
The $I(V_{sd})$ traces measured on devices on the chips that had been milled for 60s or 70s, still showed Schottky-like behaviour. This indicates that the oxide has not yet completely been removed. However, the devices that had been milled for 80s showed the linear $I(V_{sd})$ behaviour indicative of Ohmic contacts. Wires that were etched for longer than that were completely etched through. Fig.26 shows the data of just one device from each chip, but the behaviour was consistent for all devices on the same chip.

Now it seems that a working recipe for the formation of Ohmic contacts on PbTe has been found: 30s O_2 plasma etch and 80s Ar milling. However, this recipe had some issues.
The standard Ar milling recipe turned out to be quite aggressive: 10s of milling time made the difference between Ohmic contacts and wires that were mostly etched through. This leaves a very small margin of error. Moreover, ion milling is well-known to lead to amorphisation of the crystal surface. Several studies have shown that the use of a lower acceleration for the ion beam, and therefore a slower etch rate, leads to a reduction of the thickness of this amorphous layer [95][96][97]. This would be beneficial for the consistency and quality of contacts that may be formed on the etched surface, as scattering on the amorphous interlayer between the metal and the crystalline semiconductor strongly influences the behaviour of the contact. Moreover, trapped charges in the amorphous layer can significantly alter the barrier height at the interface. In conclusion: both the contact formation, and transport properties of the would benefit from the development of a less aggressive ion milling recipe.

Furthermore, the fabrication process using this milling step has a low yield of operational devices. About three quarters of the devices on each chip worked at room temperature. However, after cooling down to 10K this number shrunk to less than a third of the devices. It was hypothesised that the contacts may have come loose due the thermal contraction of the metal contacts while the sample was cooled down. This seemed plausible because gold sticks notoriously badly to other materials: the Ti adhesion layer was apparently not sufficient to prevent this detachment of the contacts.
To test whether the contacts actually came loose, or the that transport was suppressed at these low temperatures due to the presence of barriers at the interfaces, the samples were heated back up to room temperature, exposed to air, evacuated and measured again at room temperature. Many contacts were indeed destroyed by cooling down the sample, in others the contact was restored. However, in this case Schottky barriers were measures on devices that previously showed Ohmic behaviour, as can be seen in fig.27. Apparently the PbTe surface underneath the contact had oxydised.

It seemed that the Ti adhesion layer was not sufficient. Therefore, in the fabrication of all samples hereafter the adhesion layer was increased from 5nm to 20nm. Then the titanium would form the actual contact. The gold on top now acted as a capping layer to prevent the titanium from oxidising, and to reduce its line resistance.

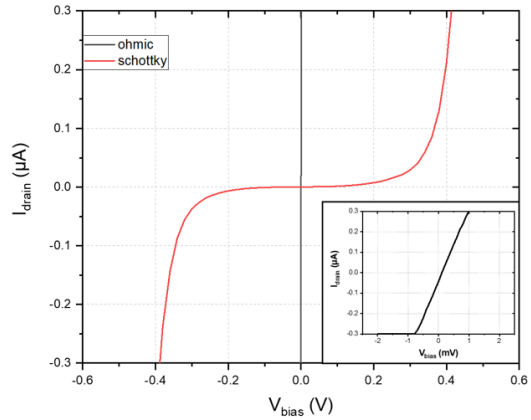


Fig. 27: $I(V_{sd})$ traces at T=10K of the same device, before and after thermal cycling and exposing the sample to air. On the first cooldown the wires showed Ohmic behaviour (black). After exposing to air, on the second cooldown the few working wires showed Schottky-like behaviour (red): the interface had reoxydised. Inset: Ohmic data replotted on a more appropriate scale.

A. *Introduction to the samples: a growth series*

Now a working fabrication recipe had been established. The contacts on all devices discussed here on forth were fabricated using the recipe described in the previous section. For the detailed recipe see chapter 4 or appendix I.

To investigate the control over doping character of the PbTe nanowires during the MBE growth, six device chips were made using nanowires with different IV/VI ratios. The growth IV/VI ratios (Pb/Te flux ratio) of this series are: The

0.799 0.802 0.880 0.941 1.01 1.14

expectation is that the doping character of the wires will change from p-type to n-type, with increasing IV/VI ratio (see chapter 2). The goal here is to verify this and quantify this doping behaviour.

B. *Schottky barrier characterisation*

First the $I(V_{sd})$ behaviour of these devices was measured at a temperature of 10K. This is measured near liquid helium temperatures to reduce the contribution to the current of thermally excited charge carriers, as these mask both the doping and contact behaviour of the wires.

Based on the results discussed before, Ohmic contacts were expected on all of the devices. However, this turned out not to be the case. As can be seen in the plot in fig.28a, clearly still Schottky barriers are formed at the metal-semiconductor interfaces.

In non-degenerately doped semiconductors, it is usually assumed that thermionic emission is the dominant transport phenomenon. Here we aim to analyse the barriers on PbTe wires with a IV/VI ratio relatively close to 1, so low doping densities ($O(10^{17}\text{cm}^{-3})$) are expected. The Schottky barrier height can be extracted from the $I(V_{sd})$ curves by fitting eq.70 to the data:

$$I_{TE} = A^{**}T^2 \exp\left(-\frac{e\Phi_B^{\text{eff}}}{k_B T}\right) \exp\left(\frac{eV_{bias}}{nk_B T}\right) \times \left[1 - \exp\left(-\frac{eV_{bias}}{k_B T}\right)\right] \tag{70}$$

This is done using a least squares fitting algorithm, which is described in more detail in appendix II. The effective Richardson constant, the electron temperature, the ideality factor, and the Schottky barrier heights are used as fit parameters. A typical fit is shown as the black dased line in fig.28.a

The fits typically match the data fairly well, except at the onset of conduction. This is because this model does not exactly match the device geometry we consider here: it describes just a single (forward-biased) barrier, while the nanowire has two contacts. However, the forward-biased injection barrier dominates the transport, as it is significantly larger than the second (extraction) barrier [59]. The reverse-biased extraction will therefore mainly contribute to the suppression of the current at low source-drain voltages. A fit of the single barrier model (eq.70) will thus overestimate the current at the onset of conduction, and further match the measured behaviour quite well.

The effective Schottky barrier heights found for all devices (at 10K) are plotted in fig.28b. A clear divide can be observed in this data: most devices have an effective Schottky barrier in the range of $\Phi_B^{eff} = 0.55 \pm 0.25$V. Taking into account the band lowering due to the Schottky effect (from eq.34: $\delta\phi = 35$mV), the actual Schottky barrier height is determined to be: $\Phi_B^0 = 0.59 \pm 0.3$V.

This is fairly close to the value predicted by the Schottky-Mott rule for a PbTe:Ti interface. The work function of titanium is $\phi_{\text{Ti}} = 4.33$eV [98] PbTe and the electron affinity of PbTe is $\chi_{\text{PbTe}} = 4.75 \pm 0.3$eV [38], so the predicted barrier height is: $\Phi_B^0 = 0.45 \pm 0.3$V. Though the calculated and the measured values are quite close, the discrepancy and the spread in the measured values implies the existance of some unpredictable surface effects (see sec.II).

One sample (IV/VI = 0.880) clearly sticks out from the rest of the data. It is quite striking that all devices on just this one sample showed such different barrier heights than all the other samples. Therefore is just as plausible, if not more, that something went wrong during the device fabrication, instead of this being a fundamental result.

To investigate SEM images of the devices from this chip were compared to images of the others. In fig.25a a SEM image of a device with a nanowire IV/VI ratio of 0.802 is shown, while the image of fig.25b shows a device with IV/VI = 0.880. It can clearly be seen that the surface of the first nanowire is perfectly smooth. This is representative for the nanowires throughout the range of IV/VI ratios investigated. However, the surface of the devices with IV/VI = 0.880 show a much rougher surface. It seems like there is some sort of droplet formation on the wire. The cause of this is unknown. But it seems likely that this will impact the interface formation, and thus the Schottky barrier height.

This phenomenon has not been observed on any nanowire device before, or since. Therefore it is assumed that some human error has occurred in the fabrication of this device. And that this device chip should not be included in any further analysis of the nanowire devices.

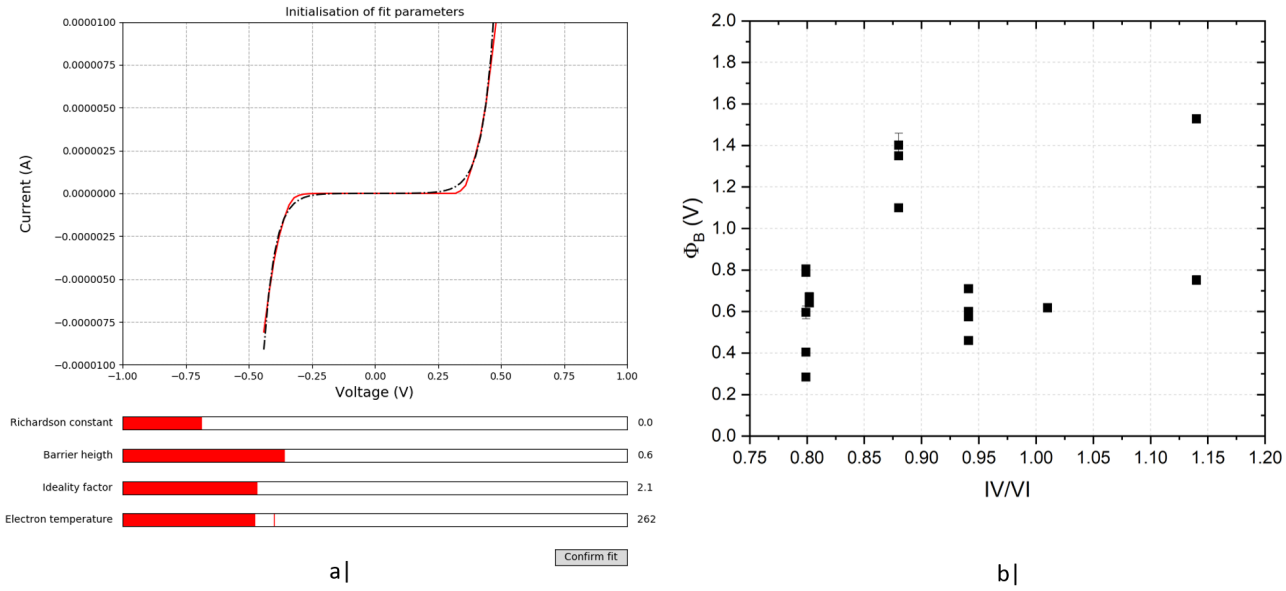
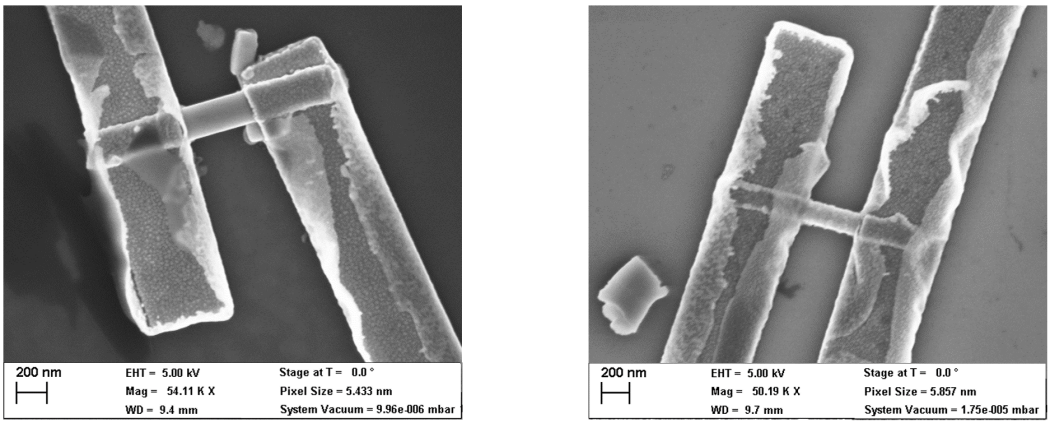
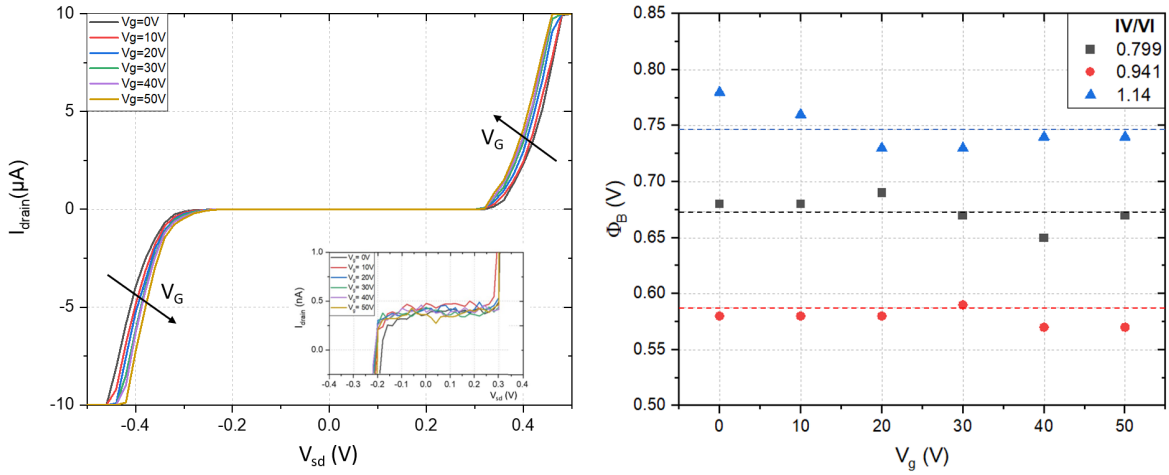


Fig. 28: Extraction of the effective Schottky barrier height:
a| Screenshot of the interface for the fitting of a curve describing thermionic emission (black dashed line) to the measured Schottky barriers (red line). The sliders at the bottom represent the fit parameters (see appendix II).
b| Plot of the extracted effective Schottky barrier height as a function of the IV/VI ratio. Except for the sample with IV/VI = 0.88, the Schottky barrier height seems to be fairly constant at $\Phi_B^0 = 0.59 \pm 0.3$V.



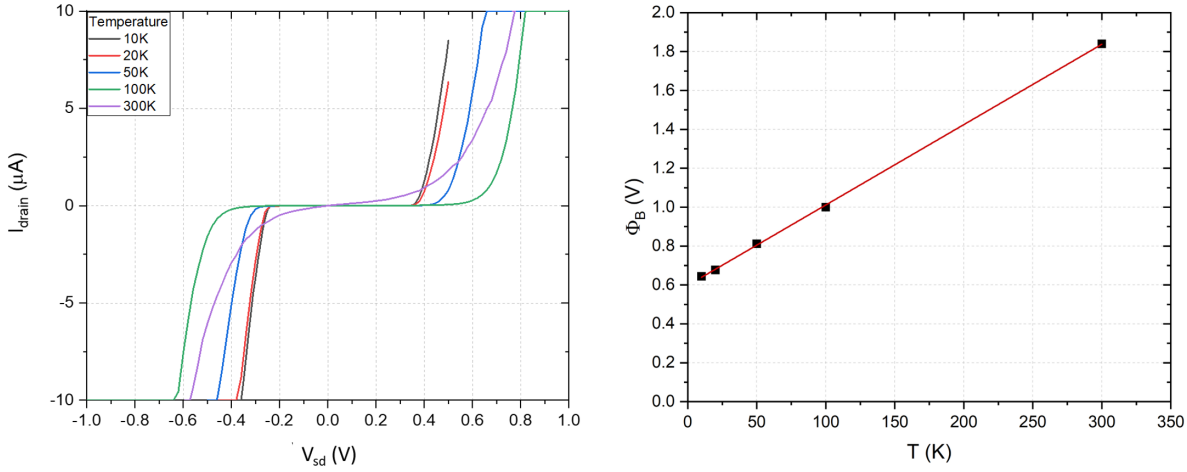
a| IV/VI = 0.799 b| IV/VI=0.880

Fig. 29: SEM image of two nanowire MOSFET devices: **a**| has a smooth surface, and is representative for most of the measured devices. **b**| has a rougher surface, and is representative for the devices with IV/VI = 0.880.



a| b|

Fig. 30: Gate voltage dependence of the Schottky barrier height:
a| $I(V_{sd})$ curves for varying gate voltages. The inset shows a close-up of the "off-regime": the measured current is in the order of tens of nano-Ampères. This is in the same order of magnitude as the noise of the measurement setup.
b| Extracted Schottky barrier heights for three devices as a function of V_g, and their average values (dashed lines).



a| b|

Fig. 31: Temperature dependence of the barrier height:
a| $I(V_{sd})$ transfer characteristics of one device for a wide range or temperatures.
b| Extracted barrier height from the curves shown in (**a**) as a function of the temperature. In red a linear fit through the data points is shown, while the dashed blue line shows the expected temperature from the modified Varshni model.

C. Gate voltage dependence

In fig.30a the $I(V_{sd})$ dependence a nanowire MOSFET is plotted for multiple gate voltages V_g. The barrier heights were determined just like before, and are plotted as a function of the applied gate voltage in fig.30b. From this plot it can be seen that the barrier heights remains constant over the range of bias voltages. This is expected, as the forward barrier does not change with the applied gate voltage.

The band bending in the wire near the interfaces (the built-in potential V_{bi}) is changed by applying a gate voltage. This does affects the height of the reverse barrier at the opposite end of the wire. This barrier only noticeably affects the conductance at the onset of the conductance regime. By applying a (positive) gate voltage the built-in potential gets reduced, thus decreasing the already small role of the reverse barrier. This explains the steeper onset of conduction, while the barrier height remains constant over a wide range of gate voltages.

D. Temperature dependence

Also the temperature dependence of the barrier height is investigated. The $I(V_{sd})$ curves for for several temperatures between 10K and 300K is shown in fig.31a. From this figure the barrier height actually seems to get wider with increasing temperature. This is the expected behaviour: the band gap of lead chalcogenides actually increases, in contrast to many other semiconductor materials. An increase in the band gap means an increase in the distance between the conduction band and the Fermi level. Therefore it also affects the band bending, which will lead to higher Schottky barriers.

It has been shown that just a linearised temperature dependence models the change in barrier height quite well for several semiconductors [99]:

$$\Phi_B(T) = \Phi_B(T=0) + \alpha_\Phi T \tag{71}$$

Here the Tersoff constant α_Φ is given by:

$$\alpha_\Phi = \frac{1}{2}\frac{dE_g}{dT}\,. \tag{72}$$

A linear fit through the extracted barrier heights yields a Tersoff constant of $\alpha_\Phi = 0.41$meV/K (see fig.31b). This corresponds nicely to the value reported by R. Dalven: $\alpha_\Phi = 0.42$meV/K [31].

Up until now only the lattice temperature of the sample has been discussed. However, eq.70 uses the electron temperature as a fit parameter to determine the Schottky barrier heights. The extracted electron temperatures are plotted in fig.32. Interestingly, the electron temperature does on average not drop far below room temperature, while the lattice is cooled to 10K. The spread in the measured electron temperatures is quite large. Again the sample with a IV/VI of 0.88 is ignored in this analysis.

At these low temperatures, phonons are mostly frozen out. Therefore the dominant mechanism for thermalisation of the electrons (electron-phonon scattering) is mostly absent. We conclude that relatively high bias voltages (up to 1V) may significantly contribute to the electron temperature.

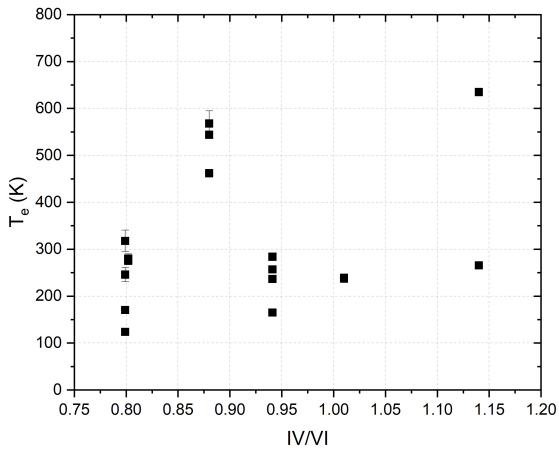


Fig. 32: Extracted electron temperatures as a function of the IV/VI ratio.

II. Transconductance and transport properties

Now we wil investigate the $I(V_g)$ transfer characteristics. It turns out that it is quite difficult to directly compare any two devices to each other, because of the fluctuations in Schottky barrier heights. These barriers directly influence the conductance. However, some qualitative statements can be made about the doping character of the devices.

The $I(V_g)$ traces at multiple source-drain voltages of a device with a IV/VI ratio of 0.802 are shown in fig.33a. To represent this data in a cleaner manner, it is replotted as the conductance (dI/dV_{sd} on a logarithmic scale in fig.33b. From this plot the actual behaviour of the device becomes a bit clearer. For low source-drain voltages the conductance decreases approximately linearly with the gate voltage. This is indicative of (subthreshold) thermionic emission of a hole current. For higher bias voltages the conduction takes on an n-type behaviour, and increases a couple of orders of magnitude.

This conduction behaviour can be explained using the band diagram of the PbTe:Ti MOSFET device (fig:34a). It is widely reported that an inversion layer forms at the interface between PbTe and a wide variety of metals [85][83][84]. This is also the case for the PbTe:Ti interface. As discussed before, this leads to barriers of $\Phi_B^0 = 0.45 \pm 0.3$eV in the valence band according to the Schottky-Mott model. This indeed explains a small subthreshold current for holes at all source-drain voltages.

The bands bend when a source-drain voltage is applied (see fig.34b). This also forms a (wide) barrier in the conduction band. The higher the applied voltage, the thinner and lower the barrier in the conduction band gets. Therefore both thermionic emission, and tunneling of electrons is expected to increase with the applied bias voltage.

This model describes a much wider, but lower barrier in the conduction band than in the valence band. Therefore tunneling is expected to be much more prevalent in the

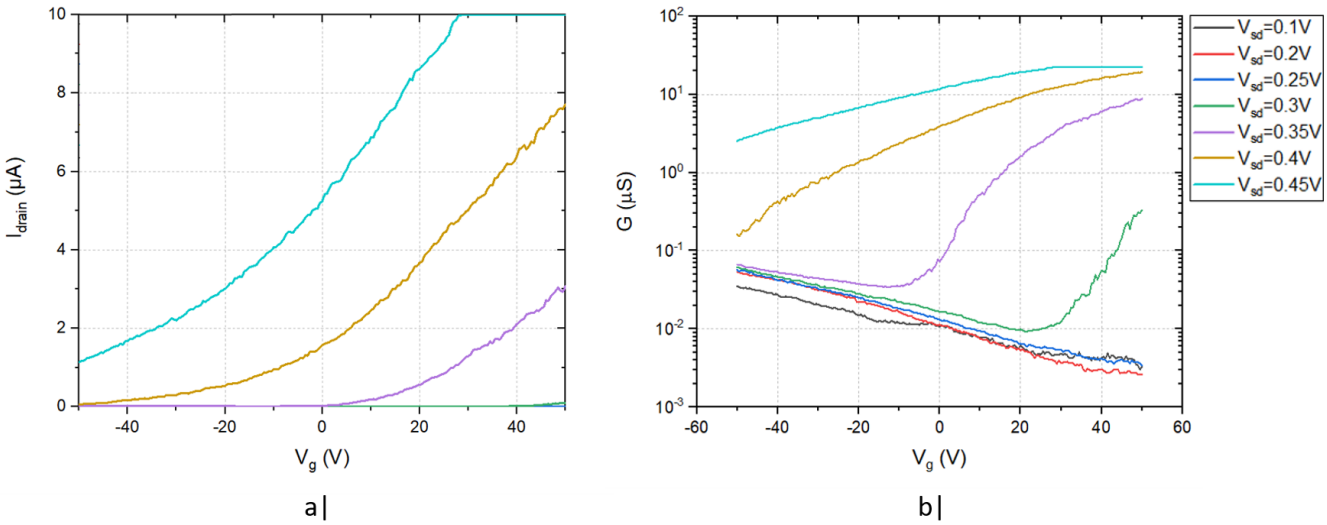


Fig. 33: Gate dependence at several bias voltages, plotted as: **a**| $I(V_g)$, **b**| $\log G(V_g)$.

valence band, and thermionic emission should be the dominant transport mechanism in the conduction band. From the data fig.33 it can be seen that the electron current is several orders of magnitude larger than the hole current. Therefore this device is considered to be n-type. The small subthreshold hole current ($O(10 - 100nA)$) is due to tunneling of thermal holes.

It turns out that this behaviour is universal for all devices: not the doping character of the wires, but the barrier formation dominates the carrier transport. There is one significant discrepancy between this model and previous results. We just established that the barrier in the conduction band is the barrier that limits the transport of the majority carriers. But this barrier is about 6 times lower than the $\Phi_B^0 = 0.59 \pm 0.3$eV that was determined before. Therefore there has to be another barrier.

Ti is more reactive with the unoxidised PbTe surface than other conventional contacting materials such as Cu, Pt and Au [100]. Photoelecton spectroscopy experiments by Lai and Cerrina et al. have actually shown that adatom exchange interactions take place at the nanowire surface [83][84]. Therefore it is likely that an interlayer is formed between the metal and the nanowire instead of an abrupt PbTe:Ti interface. This can act as an additional barrier, or completely change the character of the surface states, thus modifying the existing barrier [70][101].

In the same studies by Lai and Cerrina et al. it was shown that PbTe:Au form nondegenerate interfaces on PbTe; the Fermi level is pinned in the band gap. This will more readily lead to the formation of Ohmic contacts.

This would also explain why the developed fabrication recipe for Ohmic contacts did not work when the Ti adhesion layer thickness got increased from 5 nm to 20 nm. Ti initially form islands during sputter deposition (Volmer-Weber growth mechanism). Especially on a rough surface (PbTe after Ar milling) this may not coalesce into a single film; the subsequently deposited Au film may locally directly contact the wire, leading to an Ohmic contact. Whereas this is definitely not possible for a Ti film of 20 nm.

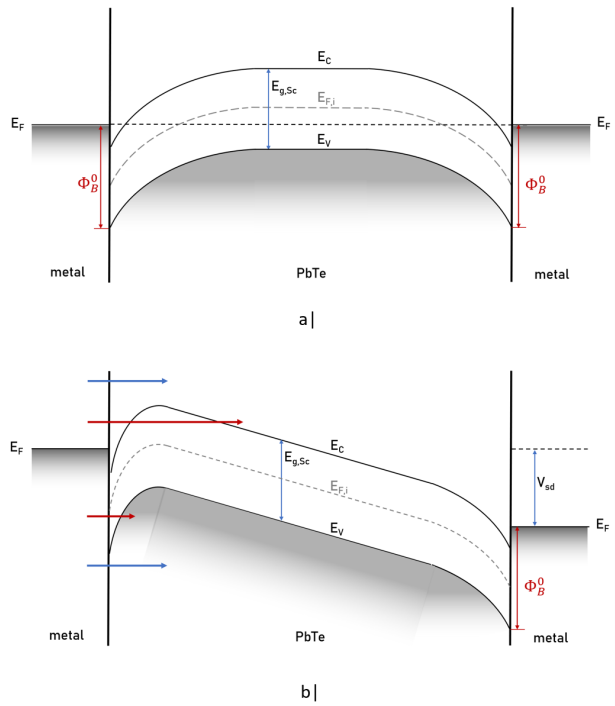


Fig. 34: Band diagram of the PbTe:Ti nanowire MOSFET:
a| without an applied source-drain voltage,
b| under forward bias. Here the red arrows indicate tunneling processes, whereas the blue arrows indicate thermionic emission.

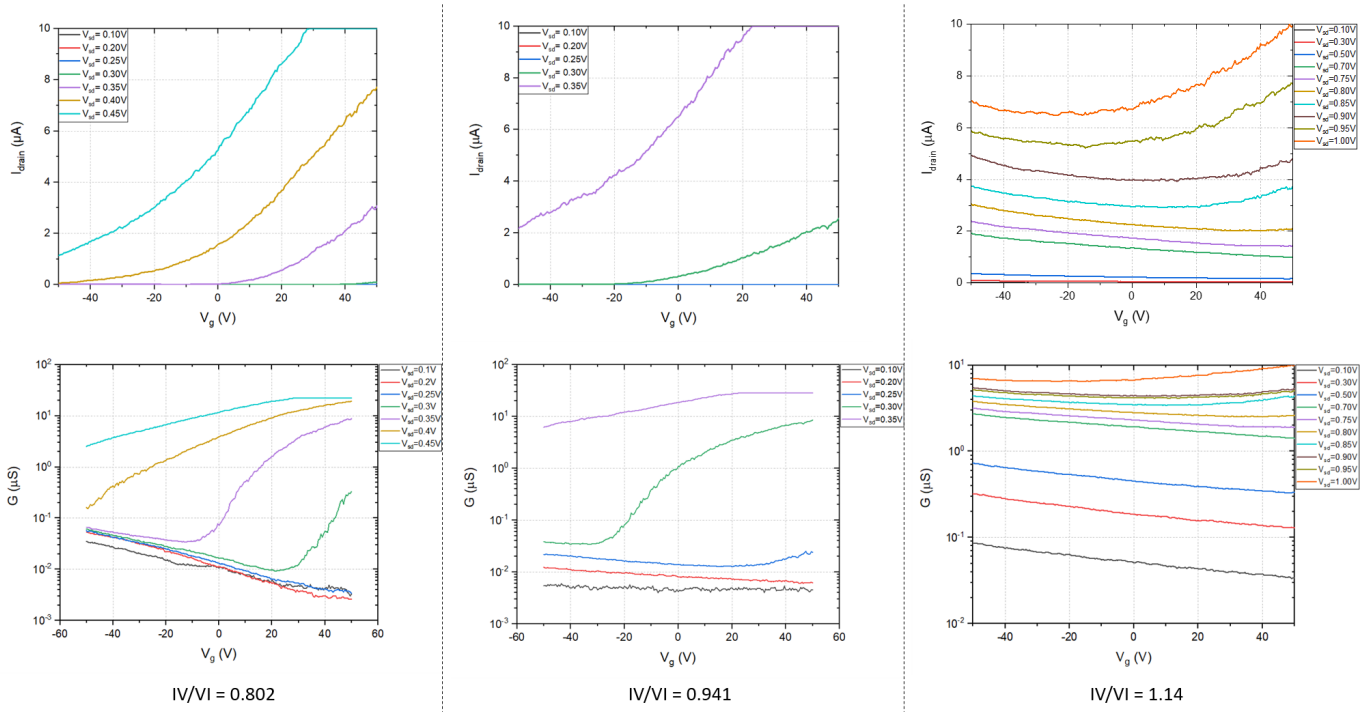


Fig. 35: $I(V_g)$ curves (top row) and log$G(V_g)$ curves (bottom row) for three devices with different IV/VI ratios.

A. Doping character

Let us now compare the gate dependence curves for different IV/VI ratios. An overview of representative $I(V_{sd})$, $I(V_g)$ and log$G(V_g)$ plots for devices of all measured IV/VI ratios is shown in appendix III. An outtake is shown in fig.35.

Because all devices have a different barrier height, again no direct comparison between the devices can be made. However, still some useful qualitative remarks can be made about this growth series.
Most useful information can be extracted from the log$G(V_g)$ curves. Let us first compare the subthreshold conductance. In a semilogarithmic plot like these, thermionic emission is linear in the applied gate voltage, whereas the conductance due to tunneling should be constant [20].With increasing IV/VI the subthreshold conductance mechanism goes from thermionic to tunneling. This, and the increase in magnitude of the subthreshold current, both indicate that the hole density increases with the IV/VI ratio.

This is corroborated by major carrier transport above threshold. The $I(V_g)$ traces for IV/VI = 0.802 and IV/VI = 0.941 are both clearly n-type. But for IV/VI = 1.14 intrinsic behaviour can be seen. It seems that the conductance behaviour due to both carrier types is approximately of the same magnitude for high bias voltages. However, this comparison cannot readily be made, because both carrier types face a different barrier. Therefore we cannot say that a growth IV/VI ratio of exactly 1.14 yields intrinsic wires. But it should be close to that value. At the very least here we have shown that the wire doping can be tuned from n-type to intrinsic by increasing the growth IV/VI ratio.

This result is a bit surprising if one looks back at fig.36. One would expect that a PbTe crystal is p-type if its composition is slightly on the Te-rich side of the ideal stoichiometry (IV/VI<1). Here we see the opposite trend. This suggests that the intrinsic point around IV/VI = 1.14 (our most Pb-rich sample) corresponds to the crossover on the Te-rich side, and all other samples further to the right. This indicates either one of two things:

- During growth Te is more readily incorporated in the nanowire. A larger Pb flux is needed to reach an actual composition of IV/VI = 1.
- The combination of the Schottky barrier and interfacial layer formation degrades the contact in such a way that any useful analysis of the nanowire is impossible. It is first necessary to optimise the contact formation before the material can be characterised at all. This will be necessary for the extraction of any relevant quantitative data as well as for future device applications.

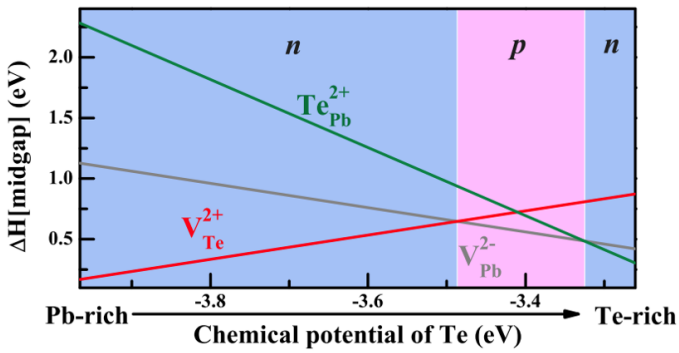


Fig. 36: Midgap formation energy for the three lowest-energy defect states as a function of the chemical potential of Te. The lowest energy defect state determines the doping character of the crystal (blue: n-type, pink: p-type). As calculated by Wang et al.[43].

Reference	Fardy et al. [47] & Jang et al. [48]	Jung et al. [51]	This work
Growth method	Chemical vapour transport method	Potentiostatical electrodeposition	Molecular beam epitaxy
Doping	n-type	p-type	n-type/intrinsic
Mobility (cm^2/Vs)	0.71-0.83	3.32	0.02-0.12
Carrier density (cm^{-3})	8.8×10^{17}	$1.85 \pm 1.06 \times 10^{18}$	$O(10^{18})$

B. Transport properties

Before we have established that the carrier transport is clearly dominated by the barriers at the metal-semiconductor interfaces. Therefore the extraction of the transport properties, as described in chapter 3, will not yield any results that are representative for the nanowires themselves. Especially the mobility is heaviliy masked by the presence of a Schottky barrier [20]. It will however give an absolute lower bound for the transport properties.

The extracted mobilities and carrier densities are displayed in the table above. As a benchmark they are compared to the transport properties reported for single-crystalline PbTe nanowires grown by other techniques. Note that the reported transport properties are extracted from a handful of devices, all with different doping and barrier heights. Therefore no meaningful standard deviation can be reported.

Transport through nanowire quantum dots

The previous chapter discussed the results obtained in Eindhoven by on the PbTe nanowire FETs. These measurements were performed at a temperature of 10K. Some of the nanowires grown at the TU/e were sent to the Frolov group at the University of Pittsburgh to be measured at cryogenic temperatures (50 mK) in a dilution fridge. These measurements resulted in some interesting results that required some theoretical study and modelling to be understood.
This chapter proposes a method to model the quantum dot behaviour seen in these nanowire devices. This model uses the configuration interaction method to describe the many-particle wave-functions in the dot, and proposed a way to calculate the eigenenergies of these many-particle eigenstates based on Wigner localised configurations. This work is far from complete, and mostly presents some qualitative results. It is just a brief foray into the world of second quantised field theories in strongly confined systems, and could best be considered a road map for further investigations. One could easily write an entire master thesis about this subject alone.

I. Cryogenic transport measurements on PbTe nanowires

Several different types of measurements were performed in the Frolov group at the University of Pittsburgh on the PbTe nanowires grown in Eindhoven. Here we will briefly discuss the relevant ones.
Similar nanowires device geometries were fabricated as the ones used in Eindhoven, with the addition of a HfO_2/Ti/Au top gate. This top gate allows for fine control of the gate voltage, which is needed for the operation of the device in the single electron transistor regime. Some small changes in the fabrication recipe allowed for the formation of Ohmic contacts on these nanowires. The most notable change is in the Ar ion milling step: a much lower etching power, and therefore a much slower etching rate is used. This is likely to result in smoother etched surfaces, and therefore cleaner metal-PbTe interfaces will be formed.

In in similar field-effect measurements the electron mobility was determined to be $\mu = 190 - 250\,\mathrm{cm}^2/\mathrm{Vs}$ at 50 mK. Also carrier densities in the order of $\sim 10^{17}\,\mathrm{cm}^{-3}$ were found. These values, while extremely high, cannot directly be compared to the numbers at the end of the previous chapter, because of the different measurement temperature. Still these are very promising results, and motivate further research in the growth and contacting of the nanowires at the TU/e.

Other interesting results is the operation of the device as a single-electron transistor. Ballistic transport through the nanowire can be observed if the thermal energy is smaller than the energy difference between the conduction channels in the dot. Because the PbTe nanowires are approximately square in cross section with a diameter of approximately $d = 80 - 100$ nm, the 1D subbands of the conduction channels can be calcuated by a simple 2D particle-in-a-box model:

$$E_{\mathbf{n}} = \frac{\hbar^2}{2m^*}\left(\frac{\pi^2\mathbf{n}^2}{d^2} + k_z^2\right) \tag{73}$$

where the subbands of the conduction channels are labelled by a vector $\mathbf{n} = (n_x, n_y)$.

So the temperature at which the first two subbands can be resolved, can be estimated to be:

$$\begin{aligned} T &= \Delta E_{\mathbf{n}}/k_B \\ &= \frac{3\hbar^2\pi^2}{2m^* d^2 k_B} \\ &= \sim 40K \end{aligned} \tag{74}$$

where the effective mass of PbTe is: $m^* = 0.034m_0$ [**?**] This behaviour is not observed in the measurements discussed in the previous chapters: while the measurements were performed at temperatures lower than 40K, the Schottky barriers prevented the observation of quantised conductance. The better quality of the contacts, and the much lower measurement temperature did allow for observation of quantised conductance in Pittsburg. However, no ballistic transport, but quantum dot behaviour was observed (see fig.37). The behaviour of the contacts at this temperature is not Ohmic: the (thin) Schottky barriers at the interfaces here form tunnel barriers between the metal and the nanowire. This defines a quantum dot in the nanowire. This phenomenon is well studied for other narrow band gap semiconductors such as InAs [102][103].

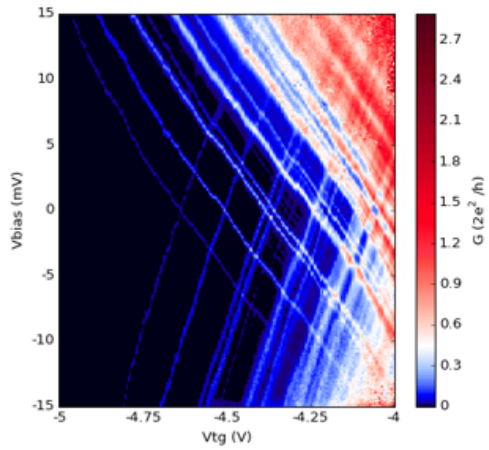


Fig. 37: Conductance (colour scale) as a function of the bias and top gate voltages. Image courtesy of E. de Jong [28]

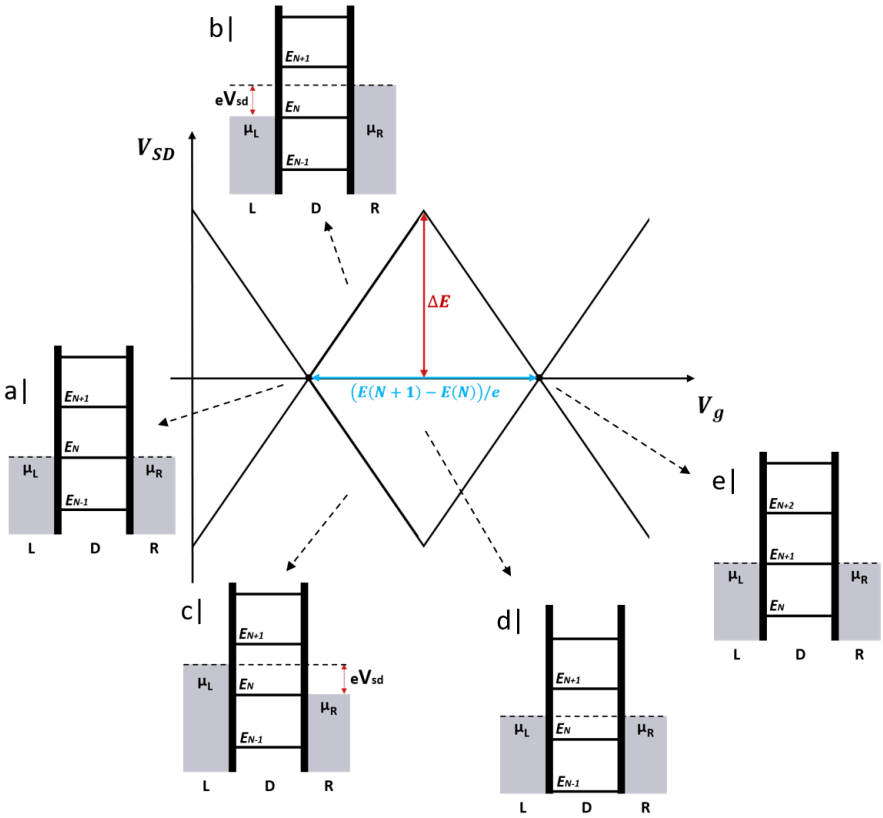


Fig. 38: Schematic depiction of a coulomb diamond. Indicated are the charging energy ΔE (red), and the gate potential required to add another electron onto the dot (blue). Around the dots some the alignments of the chemical potentials in the leads ($\mu_{L(R)}$), and the energy levels in the dot are indicated, which correspond to certain positions on the edge of the diamond.

Fig.37 is obtained by tuning the dot to the flat-band regime: no majority, nor majority carriers are present in the dot. This is achieved by applying a gate voltage of $V_g = 15V$ to the back gate. Then the top gate, and source-drain potentials can be used to open up single conduction channels in the dot. However, the wire is isolated from the source and drain leads by tunnel barriers (Schottky barriers). Therefore electrons are localised on the dot. Therefore it will cost energy to add multiple electrons onto the dot. Both the quantum mechanical level spacing, and the coulomb repulsion between the electrons themselves, will contribute to the so-called charging energy ΔE to put an additional electron on the dot.

This charging energy will now dominate the transport through the dot. This is sketched schematically in fig.38. **a**| shows the situation where the chemical potential of both the source and the drain are perfectly lined up with the Nth level in the dot. In this situation tunneling through the dot is possible: a current will flow. By changing the gate potential the "ladder"of electronic states will move up or down with respect to the chemical potentials of the contacts. Applying a bias voltage will shift the chemical potentials with respect to each other. Conduction through the dot is only possible if the level in the dot is positioned in between the two chemical potentials.
The sides of the diamond describe the edge of this conduction regime: a dot level lines up perfectly with the chemical potential of one of the leads (see **b** and **c**). Inside the diamond, both chemical potentials line up in the same gap between two levels in the dot: no conduction is possible (**d**).

The behaviour of the dot can be split into two regimes based on the (dominant) origin of the charging energy: if quantum mechanical effects dominate the charging energy the system we speak of a quantum dot. If the Coulomb repulsion dominates, the charging energy is dominated by classical effects: the system is an isolated dot, but not a quantum dot. The (Coulomb) diamonds that results from such a classical dot are have a constant shape/size: the charging energy is determined by the capacitive coupling between the dot and the source, drain and around it. The energy levels of quantum dots are generally much more irregularly spaced [104][105].
So the behaviour of the dot depends on the confinement and the electron-electron interactions on the dot. In our case it is difficult to say beforehand which effect will be dominant. The dot is relatively large: $\sim$ 100nm in diameter and $\sim$ 270 nm in length. But PbTe also has an extraordinarily large Bohr radius (46nm [52]), and will therefore show significant confinement effects in relatively large dots. Due to the extremely high dielectric constant ($\epsilon_r = 1350$ at 4.2K [106]), also the Coulomb repulsion between the electrons will be screened quite well.

Based on the consistent size of the diamonds, one would say that the device behaves as a (semi-)classical dot. However, this does not explain all the fine structure seen in the data, such as the splitting between the second and third diamonds, or the conduction resonances *inside* the third an fourth diamonds at zero bias. A proper quantum mechanical description will be necessary to fully understand the transport behaviour of the dot.

II. Configuration interaction model

Here we will start to develop a fully quantum mechanical theory of transport through nanowire quantum dots. Because the electron density is so low in the quantum dot we cannot describe electron-electron interactions using a mean-field theory. Especially not because these interactions are of vital importance for the understanding of the energy spectrum of the dot.

To properly calculate the electron-electron interactions that are so important here, a many-body quantum theory is necessary that explicitly includes the interactions between the individual particles. The configuration interaction method is well suited for problems like this, provided that the number of particles is not too large. This method builds up the many-body states of the dot from all possible configurations of single-particle states [107]. Thus the computation power needed blows up with the number of particles in the system. However, we are only interested in low occupation numbers: that is where the interesting signatures in fig.37 are observed. That is why the configuration interaction method is the method of choice for problems like this [108][]Kirstinblabla.

Some notable papers that use this method to describe quantum dot systems are written by Destefani and Marques et al. [108][109], and by Häussler, Kramer and Weinmann and colleagues [110][111][112][113][114]. One of the papers by Destefani et al. [108] modelled electronic transport through a spherical InSb quantum dot. This paper in particular has been an important guideline and benchmark throughout this work.

A. The quantum dot Hamiltonian

Let us start by examining the second-quantised Hamiltonian of the system. The Hamiltonian can be separated in a unperturbed term H_0, and a tunneling Hamiltonian for both the left and right leads $H^T_{L(R)} = H^T_R + H^T_L$: $H = H_0 + H^T$. The unperturbed Hamiltonian describes the isolated components of the dot separately: the isolated dot, the left and right metallic leads ($H_{L/R}$, and a phononic thermal bath (H_{ph}). The Hamiltonian of the dot is given by:

$$\begin{aligned} H_D = &\sum_{\alpha,\sigma} (\epsilon_\alpha - eV_g) c^+_{\alpha,\sigma} c_{\alpha,\sigma} \\ &+ \frac{1}{2} \sum_{\alpha_1,\alpha_2,\alpha_3,\alpha_4;\sigma_1,\sigma_2} \langle \alpha_1, \alpha_2 | V_{ee} | \alpha_3, \alpha_4 \rangle \\ &\times c^+_{\alpha_1,\sigma_1} c^+_{\alpha_2,\sigma_2} c_{\alpha_3,\sigma_1} c_{\alpha_4,\sigma_2} \end{aligned} \tag{75}$$

with ϵ_α the eigenenergies of the dot, $c^+_{\alpha,\sigma}(c_{\alpha,\sigma})$ the creation (annihilation) operators of an electron in state α with spin σ, and V_{ee} the electron-electron interaction. The first term here describes the energy of the individual particles: it sums over the occupied energy levels, which can be shifted by the gate potential V_g. The competing term is the electron-electron interaction: this term sums over all pairs of electrons, and calculates their mutual interaction. A first order Feynman diagram for this interaction is sketched in fig.39.

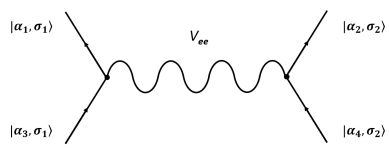


Fig. 39: Feynman diagram of the electron-electron interaction. The interaction is symbolised by V_{ee}, and $|\alpha_i, \sigma_j\rangle$ indicate the single-particle states in the dot.

The leads are modelled as a Fermi sea, with all states up to the chemical potential occupied:

$$H_{L(R)} = \sum_{\mathbf{k},\sigma} \epsilon^{L(R)}_{\mathbf{k}} c^+_{L(R);\mathbf{k},\sigma} c_{L(R);\mathbf{k},\sigma} \tag{76}$$

Where $\epsilon^{L(R)}_{\mathbf{k}}$, and $c^+_{L(R);\mathbf{k},\sigma}(c_{L(R);\mathbf{k},\sigma})$ are the energy states and creation (annihilation) operators with wave vector $\mathbf{k}$ and spin σ, in the left (L) and right (R) leads.

The coupling between the leads and the dot is described by the tunneling Hamiltonians:

$$H^T_{L(R)} = \sum_{\mathbf{k},\alpha,\sigma} \left[T^{L(R)}_{\mathbf{k},\alpha} c^+_{L(R);\mathbf{k},\sigma} c_{\alpha,\sigma} + T^{L(R)*}_{\mathbf{k},\alpha} c^+_{\alpha,\sigma} c_{L(R);\mathbf{k},\sigma} \right] \tag{77}$$

with $T^{L(R)}_{\mathbf{k},\alpha}$ the probability for an electron in state $|\mathbf{k}, \sigma\rangle$ in the left (right) lead to tunnel to state $|\alpha, \sigma\rangle$ in the dot.

Destefani et al. or Haussler et al. would now usually introduce a phonon bath with a Fröhlich electron-phonon interaction. However, we will ignore electron-phonon interactions for the rest of this report. Of course this is not entirely physical, but we are interested in modelling a system at a temperature of 50 mK. In such a system the influence of electron-phonon interactions in negligible.

B. Many particle eigenstates

Here we will discuss the construction of the many-particle states from which the configuration interaction model derives its name.

Consider a system with N particles divided over $n > N$ single-particle states. This can be done in $\binom{n}{N}$ configurations [107]. Because the fermions are indistinguishable particles, the N-particle wave function for a specific configuration can be expressed as a Slater determinant of the single particle states: [115]

$$|\phi_N\rangle = \frac{1}{\sqrt{N!}} \begin{vmatrix} \varphi_1(x_1) & \varphi_2(x_1) & \dots & \varphi_N(x_1) \\ \varphi_1(x_2) & \varphi_2(x_2) & \dots & \varphi_N(x_2) \\ \vdots & \vdots & \ddots & \vdots \\ \varphi_1(x_N) & \varphi_2(x_N) & \dots & \varphi_N(x_N) \end{vmatrix} \tag{78}$$

This state is properly antisymmetric, as any fermionic state should be. The total wave function of the N-particle state $|\Psi_N\rangle$ can now be described as a linear combination of all these Slater determinants:

$$|\Psi_N\rangle = \sum_i c_i |\phi_{N,i}\rangle \tag{79}$$

Because this many-particle state explicitly contains all possible configurations of the individual particles, it is extremely useful for the calculation of correlation effects between the electrons. The difficulty of the calculation increases rapidly with the number of particles though.

C. Transition rates: transport equations

In sec.II-A we ignored all electron-phonon interactions. This means that transport through the dot is entirely due to tunnelling. The transition probability per unit time for a particle to tunnel into or out of the dot is given by Fermi's golden rule:

$$\gamma_{i\to f} = \left(\frac{2\pi}{\hbar}\right) |\langle\Psi_f^{(0)}| H_T |\Psi_i^{(0)}\rangle|^2 \delta(E_f^{(0)} - E_i^{(0)}) \tag{80}$$

Where $\Psi_i^{(0)}(\Psi_f^{(0)})$ are the initial (final) states of the total system, with eigenenergies $E_i^{(0)}(E_f^{(0)})$.

The total effective transition rate $\Gamma_{I,J}^{L(R)}$ between two states of the dot (I and J) can then be expressed as the thermal average of the sum over all final states of the electrons in the lead. This basically is a weighted average of the total transition rate based on the likelihood that a tunneling electron ends op in a certain state in a lead. This thermal averaging reduces the Hamiltonian of the leads (eq.76) to a classical particle distribution: the Fermi-Dirac distribution $f_{L(R)}(E)$, and the density-of-states of the metal $\rho_{L(R)}(E)$ are introduced.
Therefore all possible transitions can be expressed as a decrease ($\Gamma_{I,J}^{L(R)-}$) or increase ($Gamma_{J,I}^{L(R)+}$) of the occupation number n of the dot by one electron:

$$\begin{aligned}\Gamma_{I,J}^{L(R)-} &= \frac{1}{2}t^{L(R)}(1 - f_{L(R)}(E))M_{I,J}^{-}\delta_{n_I,n_J-1}\\ \Gamma_{J,I}^{L(R)+} &= \frac{1}{2}t^{L(R)}(f_{L(R)}(E))M_{J,I}^{+}\delta_{n_J,n_I+1}\end{aligned} \tag{81}$$

with $t^{L(R)}$ a renormalised transmission rate:

$$t^{L(R)} = \frac{2\pi}{\hbar}|T^{L(R)}|^2\rho_{L(R)}(E) \tag{82}$$

here for simplicity it is assumed that the tunnel probability is independent of the quantum numbers of the tunneling electron: $T_{\mathbf{k},\alpha}^{L(R)} = T^{L(R)}$.
The Kronecker deltas are introduced to enforce that only first-order tunneling processes are allowed (only single-particle tunneling).

Now one term remains in 81 that has not yet been discussed: the matrix elements $M^{-/+}$.

$$\begin{aligned}M_{I,J}^{-} &= |\sum_{\alpha,\sigma}\langle\Psi_I| c_{\alpha,\sigma} |\Psi_J\rangle|^2\\ M_{J,I}^{+} &= |\sum_{\alpha,\sigma}\langle\Psi_J| c_{\alpha,\sigma}^{+} |\Psi_I\rangle|^2\end{aligned} \tag{83}$$

These describe the actual addition/removal of a particle from the dot. All interesting physical phenomena such as the selection rules for the transport processes are determined by these matrix elements.

The occupation probability P_I of an state I is described by the following master equation [116]:

$$\frac{dP_I}{dt} = \sum_{J,I\neq J}(\Gamma_{J,I}P_J - \Gamma_{I,J}P_I) \tag{84}$$

with $\Gamma_{I,J}$ the transition rate from a state I to a state J. Of course here a normalisation condition $\sum_I P_I = 1$ applies. The steady state occupation of a state $\bar{P}_I$ can be found by setting the master equation to zero.
Now finally the tunnel current through the dot can be expressed as the change in the steady occupation:

$$I^{L(R)} = \mp e\sum_{I,J\neq I}\bar{P}_I(\Gamma_{I,J}^{L(R)-} - \Gamma_{J,I}^{L(R)+}) \tag{85}$$

Now the framework of this model is clear, let us recap what the required ingredients for this model are:

- Energy spectrum of the dots: The eigenstates of the dot Hamiltonian. In the next section we will elaborate on this point.
- The many-body eigenstates of the dot for all relevant occupation numbers of the dot.
- Tunnel probabilities $T^{L(R)}$ can be determined from the transport data in fig.37 using the Landauer formula [116].
- For most of the commonly used contacting metals, plenty of literature can be found on the density of states of the metal $\rho_{L(R)}(E)$.

III. Energy spectra of quantum dots

The first step in the modelling of the system above is the definition of proper many-body eigenstates of the system. Let us first briefly discuss the model for the spherical InSb dot investigated by Destefani et al. Due to the spherical symmetry of the dot and the single-particle eigenstates it is natural to describe the states within the LS coupling scheme. The many-particle eigenstates are expressed as linear combinations of Slater determinants of single-particle states ($|n,l,m_l\rangle \otimes |s,m_s\rangle$) times the appropriate Clebsch-Gordan coefficients for angular momenta coupling. The Coulomb interaction is expressed as a multipole expansion in spherical coordinates, so it has the same symmetry as the defined eigenstates [117].
Using these eigenstates and the interaction terms the eigenenergies of the the dot were calculated for an occupation number of 1 to 3 particles. A Zeeman term was included in the dot Hamiltonian.

The first step in the development of our own model for the PbTe nanowire quantum dot, the model by Destefani et al. was replicated to develop the basis of the model.
These calculations were performed using the SNEG library for Mathematica [118][119]. This package allows for symbolic calculations in the second-quantised framework. This package comes highly recommended, as working symbolically helps to keep oversight over your calculations.

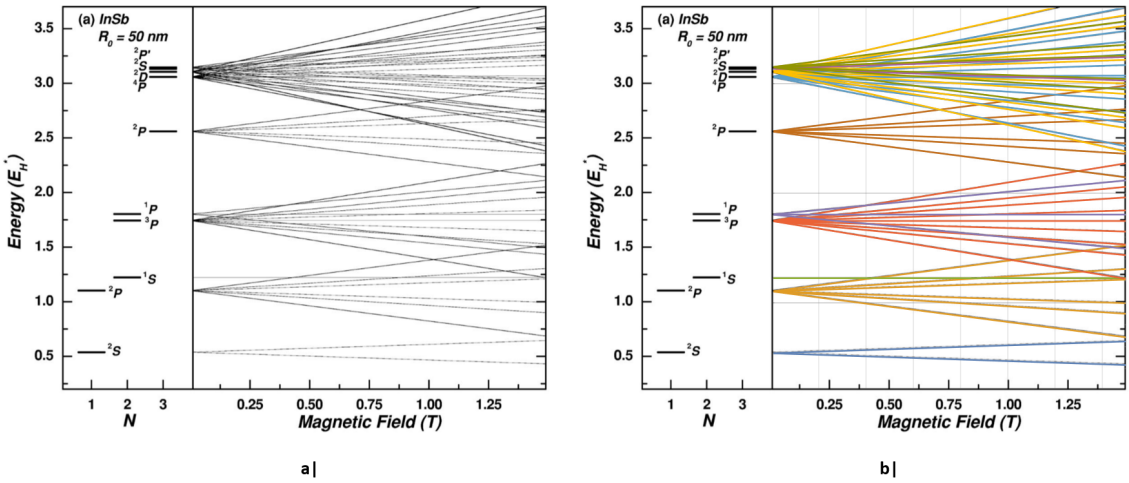


Fig. 40: Energy spectrum of a spherical InSb quantum dot as a function of an applied magnetic field.
(a) Results published by Destfani et al. [108]
(b) Replication of these results using the Mathematica/SNEG model.

And the package is equipped to deal with (anti-)commutation relations, Grassmann-valued fields, and other headache-inducing quirks of fermionic quantum field theories.
The quantum dot spectra calculated by Destefani et al. and the replicated Mathematica/SNEG model are plotted next to each other in fig.40. They are clearly in quite good agreement with each other. The energy levels are indicated in spectroscopic notation ^{2S+1}L. Due to the parallels between the eigenstates of a spherical quantum dot and atomic orbitals, the energy is plotted in units of the effective Hartree energy $E_H^* = e^2/a_B^* = 21.4$ meV, with the Bohr radius $a_B^* = \epsilon\hbar^2/(m^*e^2) = 67.1$ nm.

However, as we have hinted at before, the eigenstates of a nanowire quantum dot are significantly more complicated than the eigenstates in a spherical dot. The model of this system has not progressed enough to show any useful results. However, we will discuss some of the difficulties that arise in modelling our device geometry.
There is one big difference between a nanowire quantum dot, and the spherical dot we have discussed before: electrons in the nanowire are only confined in two dimensions. Therefore the nanowire behaves as a quasi-1D electron island. The main difficulty here is that electrons in this dot do not necessarily have a fixed position, as would be the case in a 0D dot, like we discussed before. This significantly complicates the calculation of interaction terms between electrons.

One phenomenon is quite important in the description of spatial distributions of low density and low temperature electron gasses: Wigner crystallisation [120][121][122]. Wigner crystallisation, or Wigner localisation in 1D, is the spontaneous formation of a crystal-like electron probability density distribution dominated by the Coulomb interaction. It can best be understood in terms of two competing energy terms: the kinetic energy of the electrons, and the Coulomb repulsion between them. If the Coulomb repulsion between the electrons is large enough to suppress their movement

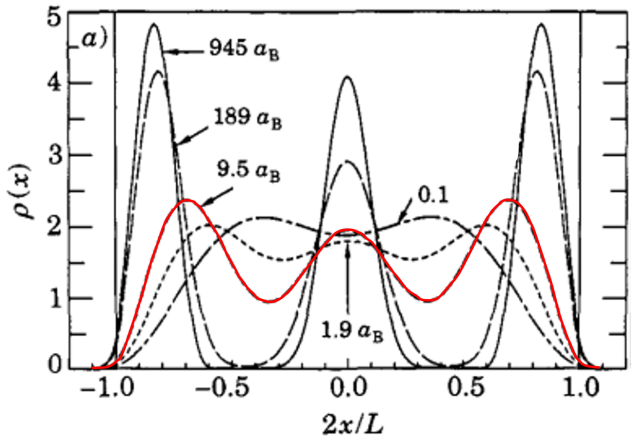


Fig. 41: Electron density probability distributions for three electrons in a dot for different nanowire lengths, plotted on a normalised x-axis. The red profile ($9.5a_B = 437$ nm for PbTe) is the closest to our channel length of 270 nm. Adapted from Jauregui et al.[120].

due to their thermal energy, the electrons will condense in a lattice.
This is shown schematically fig.41 for three electrons in wires of different lengths. Longer nanowires allow for the full separation of the electrons, while the localisation is suppressed for shorter wires/higher electron densities. The red curve is closest to our nanowire quantum dot device.

Let us now consider just two electrons in the nanowire quantum dot, to further understand this Wigner localisation. Two limiting cases can be imagined:

- **Weakly interacting particles**. Two weakly interacting particles will not repel each other, and therefore not form a localised state. The first two single-particle states form a singlet and are therefore degenerate in energy. The excitation spectrum of the dot is dominated by the subband splitting due to the confinement. Therefore the 1-particle and 2-particle excitation energies will be the same [121].

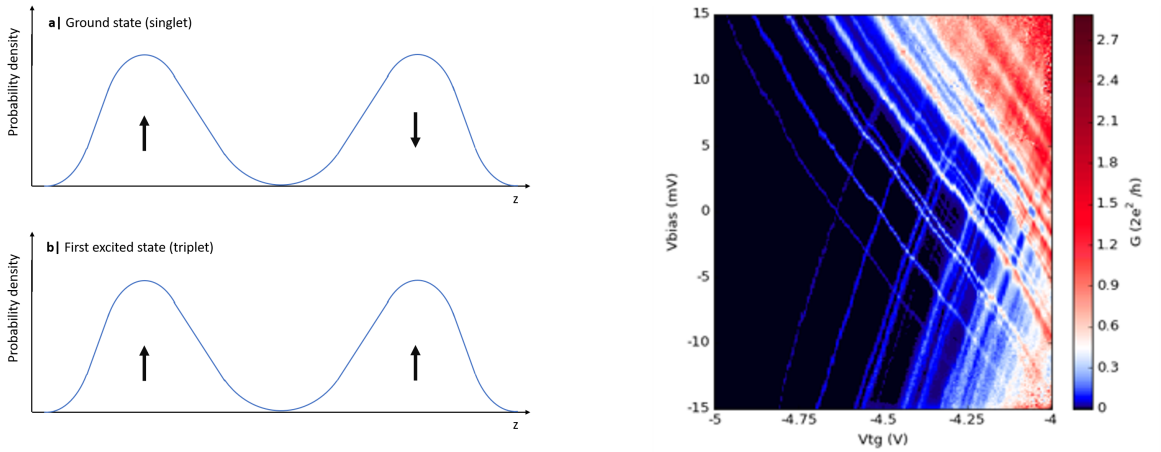


Fig. 42

- **strongly interacting particles** Two strongly interacting particles will localise on opposite ends of the nanowire (see fig.42a). The two particle ground state will form a singlet. However, the first excited state will now be a triplet state see fig.42b), not the next subband. The energy splitting between the singlet and the triplet states is quite small because the single-particle states barely overlap.

This is exactly what we see in the data in fig.42(right). The second electron that enters the dot can have a spin state that either forms a singlet or a triplet state with the electron that is already in the dot. Both will have a slightly different charging energy, ad thus a slightly differently sized diamond. This is explains the splitting of the edges of the second diamond at zero bias. The ”splitting” is actually the overlap of two sightly differently sized diamonds for the second electron in the dot, each corresponding to one spin state. This is a signature of Wigner localisation in the quantum dot.

To properly quantify this claim, the interaction energies and the phase transition to the Wigner localised phase can best be modelled using a bosonisation approach: the system can then be described as a 1D Luttinger liquids of non-interacting bosons [123][124])[125]. This is an effective field theory that is commonly used for the description of complex phenomena in one-dimensional systems. The bosonisation procedure is quite daunting, and is far from in a finished state right now.

Concluding remarks

Here we will conclude this thesis by recapitulating the main results. Lastly some recommendations for follow-up research, future lines if inquiry and Other general advice is given.

Sinlge-crystalline PbTe nanowires have been grown using MBE. To characterise the electrical properties of these nanowires, they were fabricated into nanowire MOSFET devices. Attempts have been made to optimise the contacts between these nanowires and metallic source and drain leads. However, Schottky barriers were formed at the metal/semiconductor interface, partially due to the choice of materials, and partially because of the the Ar milling process used during the fabrication.

These Schottky barriers have been characterised based by fitting the measured $I(V_{SD)}$ curves with a formula describing thermionic emission. From the quality of this fit it is determined that thermionic emission is the dominant transport mechanism in through the nanowire MOSFET. The barrier height has been determined to be $\Phi_B^{\text{eff}} = 0.55 \pm 0.25$V. This value has been obtained independent of the doping (IV/VI ratio) of the wire, which indicates some degree of Fermi level pinning.

Despite the Schottky barriers, an attempt has been made to extract the carrier mobility and density from the measured $I(V_G)$ data. Carrier densities in the order of $\sim 10^{18}$cm^{-3} have been obtained. This seems a plausible value compared to the carrier densities of other narrow band gap semiconductors (InAs, InSb). The obtained mobilities ($\mu_e = 0.02 - 0.12$cm^2/Vs) are two orders of magnitude lower than in other semiconductors. However, it was to be expected that the mobility of the device was heavily impacted by the presence of barriers at the contact interface. Hopefully the contacting can be optimised soon, so the actual material properties of the wire as a result of the MBE growth conditions can be probed.

Cryogenic transport measurements were performed on similar devices in the Frolov group at the University of Pittsburgh. The barriers at the metal/semiconductor interface, though much less pronounced, turned the nanowires into nanowire quantum dots. Some curious signatures were observed in the transport characteristics of these dots. Some of these features can be explained to be signatures of Wigner localisation of electrons in the dot. Steps have been made in the full quantum-mechanical modelling of this system, but still a lot of time has to be invested to completely reproduce the experimental results.

I. Fabrication of PbTe devices

A first recommendation might not be too surprising: develop a Ar milling recipe that is less intrusive. Our own results already suggested that this is a major issue in the formation of proper Ohmic contacts on the PbTe nanowires. And this is more substantiated by the fact that the Frolov group in Pittsburgh was actually able to create Ohmic contacts using a lower Ar etch rate.

In the mean time some further progress was made in the development of a suitable etching process in our labs. In fig.43a shows an SEM image of a nanowire etched with the old recipe. This surface is very rough, and a significant part of the nanowire is etched away. Compare this to fig.43b, which shows a trial with a Ar milling recipe with reduced acceleration voltage and etch rate. This wire was partially covered with PMMA during the erching process. It is clearly visible that the uncovered (left) part of the wire is etched, while the other half is not. However, significantly less of the wire is etched away and the syrface looks quite smooth. Whether this will lead to the formation of Ohmic contacts has to be tested by actually fabricating and measuring a device.

Still it might be interesting to also investigate other materials for the contacts. Here was chosen for Ti/Au because it is a fairly standard contact material combination for nanowire devices. However, there are plenty of other material options and fabrication techniques that can yield Ohmic contacts.
For example: Ti/Au contacts are also known to form Schottky barriers in the valence band on InAs. However, Ford et al. report that annealing of these contacts can result in the formation of Ohmic contacts [63]. This seems to work as well with other metals [126]. However, with an eye on future research it might not be a great idea to develop a recipe that relies on annealing for proper contact formation. For Majorana experiments it will eventually be necessary to have both normal and superconducting contacts on the same nanowire. The superconductor of choice for PbTe is Pb. Unfortunately dewetting of the Pb is expected at the temperatures needed for annealing of the conventional contacts.
Another option might be to seed a gold contact using a galvanic displacement reaction prior to e-beam evaporation to form Ohmic contacts. A method proposed by Jung et al. [51] submerges the substrate with oxidised PbTe nanowires (and an exposed and developed PMMA mask) in a gold-plating solution. After several hours gold nanoparticles will have formed directly on the PbTe. Now only gold has to be deposited using e-beam evaporation for the formation of Ohmic contacts.

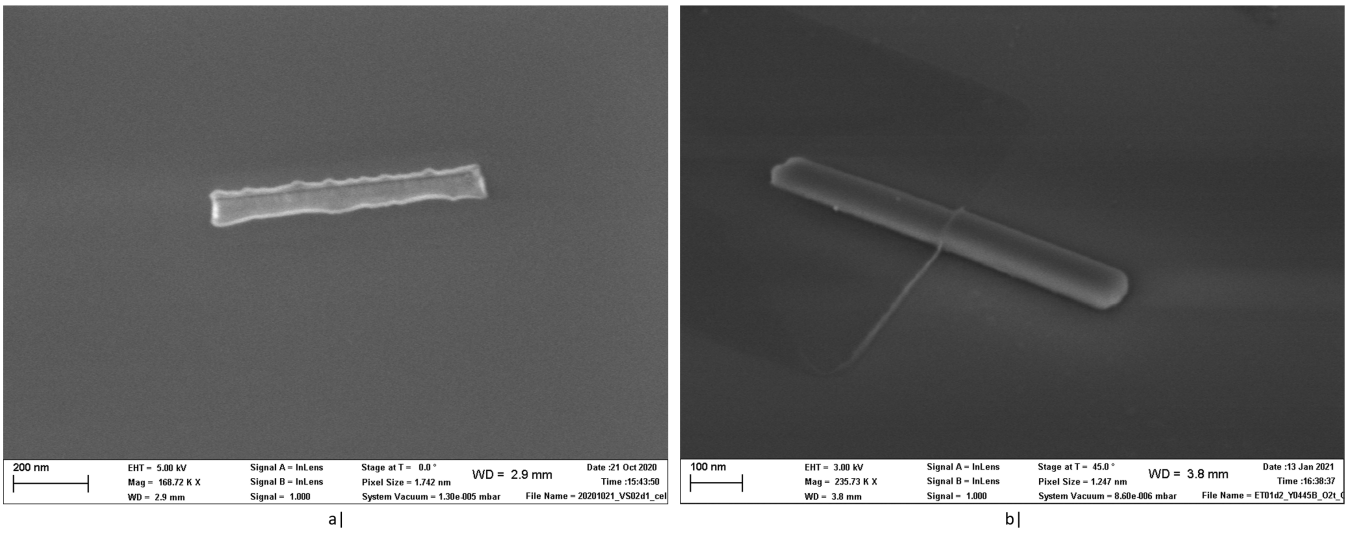


Fig. 43: Scanning electron microscopy images of PbTe nanowires etched with the ols (**a**) and adapted (**b**) Ar milling recipes. Image courtesy of Vince van de Sande.

It might also be interesting to investigate other materials for the formation of different contacts. Some may result in the formation of Schottky barriers in the valence band, others in the conduction band. The height and character of the barrier can be determined by a proper choice of contact materials. However, we have seen before that the Schottky-Mott rule does not properly predict the formation the barriers formed by a specific material combination.
A better way to predict might be a model by Baldereschi and Monch [127][128], as it explicitly includes the occupation of surface states [70]:

$$\Phi_B = \Phi_{bp} - S_X(X_m - X_{sc}) \tag{86}$$

Where Φ_{bp} is the branch point energy with respect to the valence band maximum, and X_m and X_{sc} are the electronegativities of the emetal and the semiconductor respectively. S_X is the so-called slope parameter (see for example [70]), which depends on the material choice. This model looks very simple. However, the best way to determine the branch point energy is from tight binding calculations of the band structure of the semiconductor material. So this is less straight-forward then it seems.

II. Improvements for measurements and data anlysis

When proper contacting of the nanowires is achieved, the measurement procedure and data analysis of the field-effect measurements can also improved. One notable improvement could be the use of a micromanipulator to transfer the nanowires, instead of the tissue transfer method. This is much more time consuming. But nanowires break in unpredictable places when transferring wit a tissue. The hope is that longer nanowires can be transferred by using a micromanipulator.
If nanowires with a length of $\sim 2\mu m$ can be transferred to the sample, they can be fabricated into 4-point FETs. This allows for the 4-point probe measurements, which can be used to determine the contact/line resistance of the measurement setup. Up until now this was not successfully done. From SEM images of the growth chips we have seen that the wires should be long enough to fit four contacts, but rarely any wires of that length make it onto the device chip. Nanowires of this length can also be interesting for the formation of quantum dots: devices with different channel lengths can be made by varying the distance between the contacts. The length of the dot determines on the overlap of the single-particle wavefunctions in the dot, and thus influences the phase transition from quantum dot to wigner molecule.

Also the data analysis can still be improved. For example, the capacitance of the devices is now estimated quite crudely. Especially the paracitic capacitance/shielding of the back gate capacitance by the source and drain leads can result is significantly altered capacitance valued. As the capacitance is a vital ingredient in the determination of the transport properties of the device, such as the mobility.
The capacitance value can be determined more precisely in one of two ways: by modelling or by directly measuring the capacitance. In the Kouwenhoven group in Delft, is chosen for the first approach: first a 3D Laplace solver is used to calculate the electrostatic potential in the nanowire. This takes all gates into account. Then a 2D Laplace solver and a 2D Schrödinger-Poisson solver are compared to investigate the contribution of quantum effects to the capacitance. The capacitance is classically completely determined by the device geometry: the spatial distribution of electrons distribute minimises the electrostatic energy of the system. Quantum effects introduce other energy terms that modify this lowest energy state, which will yields a different capacitance value. From the comparison of the 2D models it is concluded that the Laplace solver overestimates the capacitance by 20%. Therefore the device capacitance is determined to be the value found fro the 3D Laplace solver, with a reduction of 20%.

The capacitance can also directly be measured in CV spectroscopy experiments. These are quite difficult to perform,

due to the small absolute values of the capacitance of the nanowire FETs ($O(10^{-17}$F). However, a method has been developed by Ilani et al. at Cornell University specifically for the application of nanowire FETs [129][130][131].
Directly measuring the capacitance has the advantage that it includes all device imperfections that are hard to model, such as imperfections device geometry due to the fabrication process, the effect of charged surface states [131], or fluctuations in the dielectric constant and thickness of the gate dielectric. This last point can especially be beneficial if multiple layers of different dielectric materials are used, such as in top gate devices.

III. Configuration interaction model

For the analysis of future experiments on ballistic PbTe nanowire/quantum dot systems, it may be useful to continue with the theoretical study of quantum dots as set up in chapter 7. It will be an extensive theoretical investigation though. However, this chapter is in itself half of an overview of the theory/an outlook. So there is not much benefit in repeating that here.

Appendices

I. Device fabrication recipe

Here the fabrication recipe for the nanowire MOSFET devices is explained in more detail. The fabrication is divided up into four parts:

1) The deposition of the global back gate
2) The patterning and deposition of the main architecture of the chip. This includes the contact pads for contacting the chip to the measurement setup, markers, and chip identifiers.
3) Transfer of the nanowires from the growth chip to the device chip.
4) The patterning and deposition of the approach contacts.

These fabrication steps will separately be discussed below.

A. Back gate contact

- All devices were created on 1×1 cm pieces of a 525 μm thick SiO_2-$n^- - Si$-SiO_2 wafer. Both thermal silicon oxide layers are 100 nm thick.
  Earlier devices have also been created on SiO_2-$p^+ - Si$-SiO_2 substrates, but none of the measurements performed on these devices are shown in this thesis. DIFFERENCE IN GATING
- A resist layer is spin-coated on one side of the substrate to protect it during the following processing steps. The resist used is 950K PMMA A11. It is spin-coated at 2000 rpm for 60 seconds, and then baked at a hotplate at 180degC for 8 minutes.
- The oxide layer on the uncovered side is removed using a CH_3H:O_2 reactive ion etch (RIE) for 7 minutes.
- The 100 nm Au contact with a 2 nm Ti adhesion layer is deposited on the bare $p^+ - Si$ side of the substrate using e-beam evaporation.
- The resist layer is removed by putting the sample in acetone for an hour or longer, and in an ultrasonic bath for a few minutes if necessary. then the sample is cleaned off with IPA and blow-dried with nitrogen.

B. Contact pads and markers

- A new resist layer (950K PMMA A6) is spin-coated on the (not gold covered) top side of the substrate. The PMMA is spin-coated at 3000 rpm for 60 seconds, and baked at a hotplate at 180degC for 3.5 minutes.
- Then electron beam lithography is used to pattern the contact pads, alignment markers and marker fields, and other identifiers into the resist. The dose used is 1500μC/cm^2.
- The resist is first developed in a MIBK:IPA 1:3 solution and then in IPA, both for 80 seconds. The sample is then blow-dried with a nitrogen gun to remove any residual IPA. This stops the development.
- Again a 2 nm Ti/100 nm Au film is deposited using e-beam evaporation. on top of the resist.
- The PMMA and residual metal layer is lifted off, by solving the PMMA in acetone. The sample is left in acetone for several hours, preferably overnight. Ultrasonication can be used to remove the gold layer if it sticks. Again the sample is cleaned with IPA and then blow-dried with nitrogen.

C. Nanowire transfer

- Nanowires are transferred from the growth substrate to the marker fields by the tissue transfer method: the tip of a piece of cleanroom tissue paper is swiped over the growth substrate. Wires will break off and stick to the tip of the paper. Then by swiping the tip over the marker fields, some wires will inevitably detach from the tissue and remain on the sample.
- The position of the nanowires relative to the marker fields can now be determined using an SEM. Based on these SEM images, a CAD design for the approach contacts can be created using KLayout.

D. Approach contacts

- Spin resist on top side. Recipe: 950K PMMA A6 at 3000 rpm 60 seconds, then bake at 180degC for 3,5 minutes.
- EBL of small contacts.
- Develop: 80 seconds in MIBK. 80 seconds in IPA. Blow-dry.
- oxygen etch
- Argon ion milling is employed to physically etch away the native oxide on the nanowire. This oxide prevents the formation of Ohmic contacts. The sample is placed at a 25 cm distance from the source. And an argon gas flow of 11 sccm was used. The Argon milling tool has a gridded ion source that uses DC discharge to generate ions. All relevant electrical parameters are shown in the table below:

V_{beam}	600 V	I_{beam}	45.9 mA
$V_{\text{accelerator}}$	119 V	$I_{\text{accelerator}}$	9.2 mA
$V_{\text{discharge}}$	40 V	$I_{\text{discharge}}$	0.43 A
V_{cathode}	7.3 V	I_{cathode}	5.97 A

- In the same system a 20 nm Ti and 20 nm Au layer were sputtered. It is important that this is done in the same vacuum system as the ion etching step, as breaking the vacuum will result in reoxidisation of the nanowire.
- An additional 100 nm of gold were deposited using e-beam evaporation. A total thickness of more than 120 nm is needed to ensure that the entire wire is capped by the approach contact. GROWTH RATE
- Resist lift-off. Acetone for 2 hours or longer, ultrasonic bath for few minutes. Clean with IPA. Blow-dry.

II. Data fitting

This appendix is meant to elaborate on the fitting procedures used. For this purpose, python scripts were written based on the curvefit function from the scipy scientific computing package. Using this function a least-squares fit of a predefined (non-linear) function can be fitted to the data.

Four fitting parameters are used to fit eq.**??** to the data: the prefactor A^{**} (effective Richardson constant times the effective interface area), the barrier height Φ_B^{eff}, ideality factor n, and the electron temperature T_e. Because the fitting function depends exponentially on three of the four fitting parameters, it is very sensitive to the initial conditions given to the fit algorithm. If the initial conditions differ too much from the actual data, the fitting algorithm does not converge.
Therefore an interface was created (fig.1a), which plots the data (red), and the initial fit function (black). Using sliders the fit parameters can be changed to approximately match the black curve to the data. These fit parameters are then used by the curvefit function to fit the fit function to the data.
Testing of the fitting script has shown that the electron temperature and ideality factor are insensitive to the initial conditions. If the fit converges, the algorithm returns the same n and T_e up to 3 significant digits, regardless of the initial conditions. This has been tested by performing 25 fits with different initial conditions on the same data set. And this has been repeated for three different data sets.
Now the fitting procedure is repeated, but with the electron temperature and ideality factor fixed on the values obtained by the initial fit. The values for the effective Schottky barrier height obtained by this second fit are used in the results section of this thesis.

Fig.1b shows the fitting interface for the analysis of the measured $I(V_g)$ curves. The linear part of a curve like this is of interest (see sec.**??**). Using the sliders the relevant fit range can be determined. Then again a least-squares fit algorithm is used to fit a linear function to the data. From this fit the transconductance and the threshold voltage of the device can be determined. These are in turn required to calculate the mobility and channel carrier density of the MOSFET device.

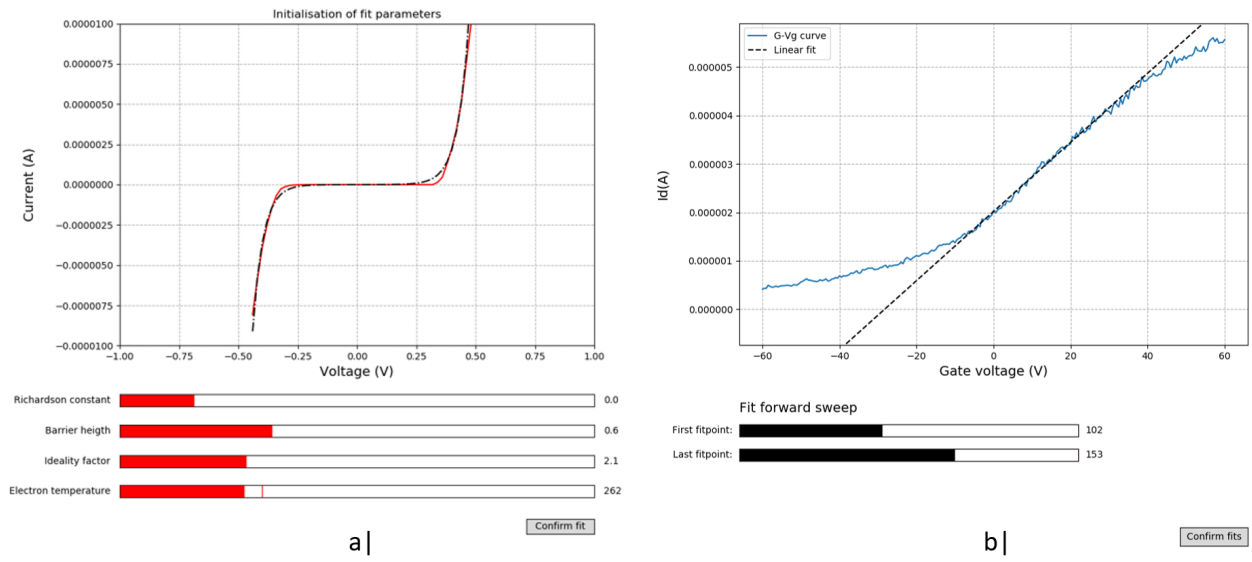
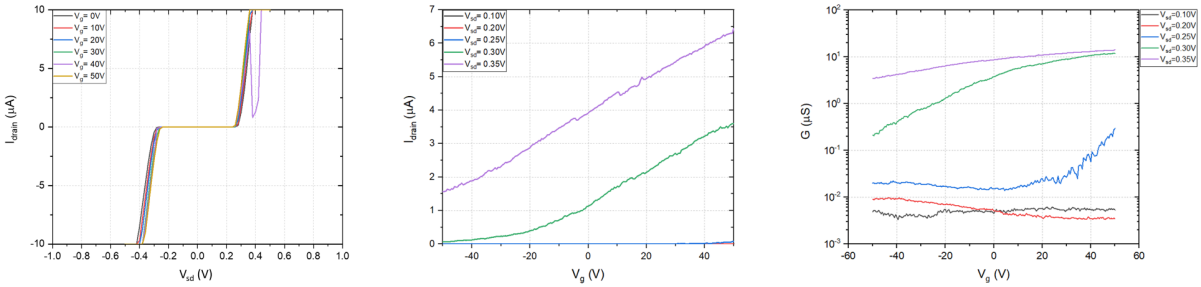


Fig. 1: Fitting interfaces. **a** plots the data (red) and the ansatz for the fit curve (black dashed line) based on the initial fit parameters chosen using the sliders. **b** shows a measured $I(V_g)$ curve (blue), and a linear fit (black dashed line) through the non-saturated part of the data. The sliders can be used to select the range of the plot through which the line is fitted.

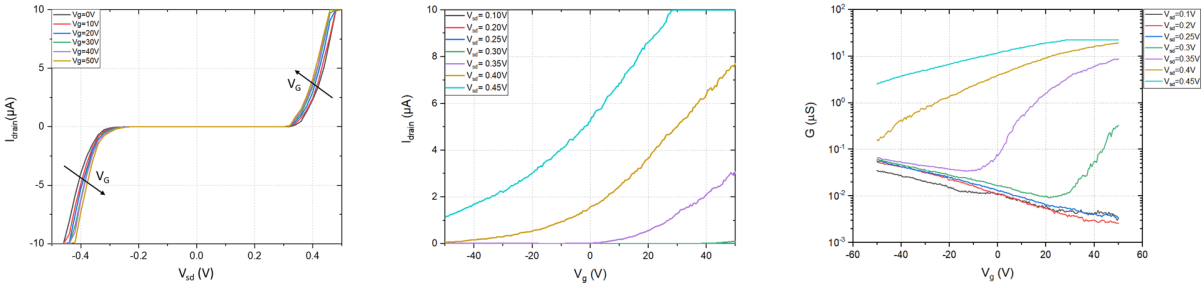
III. Supplementary data

On the next page the $I(V_{sd})$, $I(V_g)$, and log$G(V_g)$ curves for representative devices from all device chips from the growth series are shown on the next page. There is a clear trend from n-type to intrinsic behaviour with increasing IV/VI ratio. A full analysis of this data can be found in chapter 6.
Notice also the unexpected behaviour for the devices with (IV/VI = 0.880).

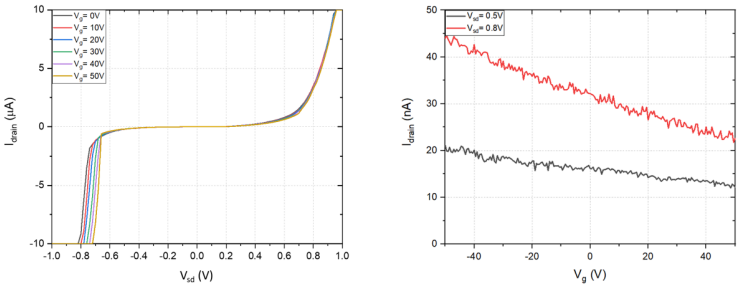
IV/VI = 0.799



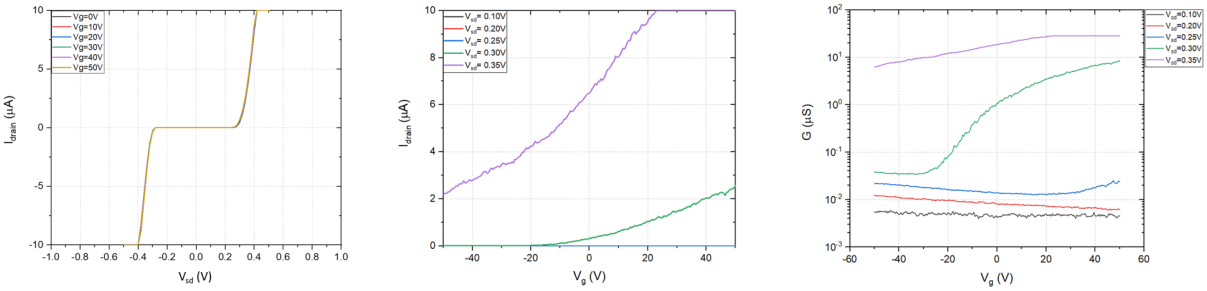
IV/VI = 0.802



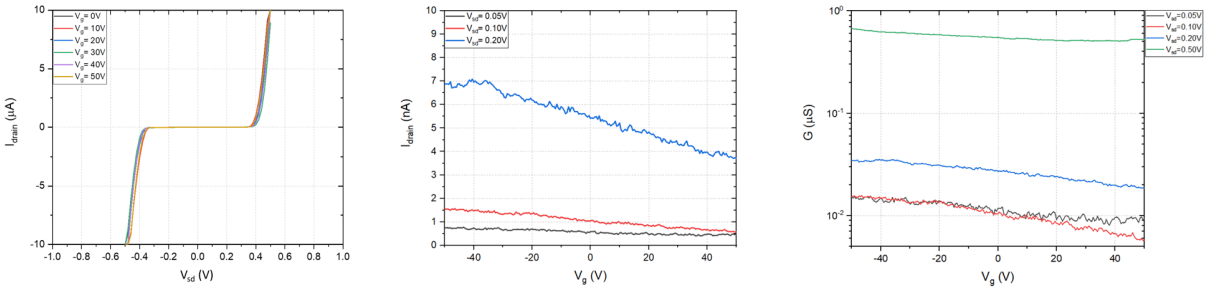
IV/VI = 0.880



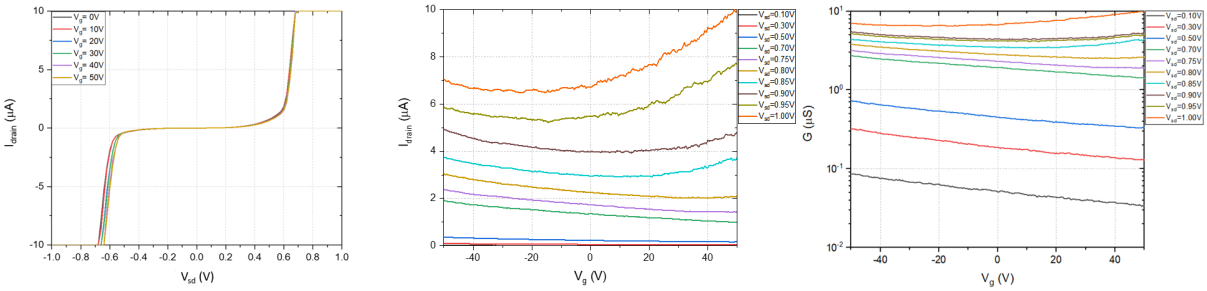
IV/VI = 0.941



IV/VI = 1.01



IV/VI = 1.14



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